PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments to belgard@umunhum.stanford.edu.

5,455,909

Microprocessor with operation capture facility
Issued: October 3, 1995
Inventors: James S. Blomgren, et al
Assignee: Chips and Technologies
Filed: April 22, 1992
Claims: 5
The invention provides a microprocessor with a special Operation Capture Facility (OCF) mechanism that enables faulting whenever there is (a) a memory access request to any one of a specified group of memory blocks, (b) a request to access any one of a group of specified I/O ports, or (c) any one of a specified group of interrupts is activated.

5,454,117

Configurable branch prediction for a processor performing speculative execution
Issued: September 26, 1995
Inventors: David L. Puziol, et al
Assignee: NexGen
Filed: August 25, 1993
Claims: 3
Branch prediction is configurable via a control line to alter the manner in which the branch prediction is generated. The configuration can be done programmatically in software or by hardware in response to processor events. Such processor events include the loading of the CS register and changes in the instruction workload.

The directions of a group of branches are predicted, based partly on resolved branch history information. Tentative branch history information is then stored for each of the predicted branches. When a predicted branch is resolved, the resolved branch history information is updated based on the tentative branch history information for the branch most recently resolved. Additionally, the predictions may be partly based on preceding unresolved branch predictions if any are outstanding.

Hit/miss information from a Branch Prediction Cache (BPC) can optionally be used in formulating the next state value of an addressed two-bit counter stored in a correlation-based branch history table. Since a miss in the BPC may indicate that this branch has not been encountered recently, whatever state currently exists can be optionally forced to a state that is based solely on whether the branch is resolved taken or not. This feature may be enabled and disabled under software control.

Information from the instruction decoder is optionally used to override the correlation-based BHT-based prediction for select branch instructions. This feature may be enabled and disabled under software or hardware control.

5,454,089

Branch look-ahead adder for use in an instruction pipeline sequencer with multiple instruction decoding
Issued: September 26, 1995
Inventors: Truong Nguyen, et al
Assignee: Intel
Filed: October 26, 1993
Claims: 6
Logic examines signals from an instruction fetch unit to determine if the next instruction is a branch. If so, a full adder adds the branch displacement to the instruction pointer. The result is used as the branch address. The timing is such that a one-clock lookahead is sufficient to hide this calculation from program execution. A branch bypass mechanism causes the branch address to be driven from the calculation instead of a branch register. If a branch failure or scoreboard hit occurs, a write cancellation is generated to stop the current address calculation from being stored; otherwise, it is stored in a branch register. If a branch bypass occurs, the branch address is driven from the calculation; otherwise, it is driven from the register.

5,454,087

Branching system for return from subroutine using target address in return buffer accessed based on branch type information in BHT
Issued: September 26, 1995
Inventors: Susumu Narita, et al
Assignee: Hitachi
Filed: October 23, 1992
Claims: 5
An address of a branch instruction, its target address, and its type are stored as branch history information in a branch instruction buffer. In addition, a return address for a return from a subroutine is retained in a return buffer. A lookup operation is conducted through the buffer by using the prefetch address such that when a hit occurs, a branch target address is output from the buffer, depending on a branch instruction type.

OTHER ISSUED PATENTS

5,454,115 *Data-driven type processor having dataflow program divided into plurality of simultaneously executable program groups for an N:1 readout to memory-access ratio*
5,454,092 *Microcomputer having an improved internal address-mapping apparatus* ♦