THE EDITOR'S VIEW

Intel's Geography Lesson

Product "Rivermap" Includes Klamath, Deschutes, and Merced

If you have seen Intel's latest processor roadmap, you know that a river runs through it. In fact, it resembles nothing so much as a whitewater rafting itinerary, listing destinations such as Klamath, Deschutes, and Merced. These code names have replaced the traditional "Pxx" nomenclature that Intel used for a decade. Recent leaks from the blue HQ have provided insight into how the waters will flow.

The Klamath River (with bodacious Class V white water, if you like to get wet) flows across the Oregon border into California, perhaps symbolic for a processor designed at Intel's Hillsboro (Oregon) site with help from the Santa Clara (California) team. Sources indicate that Klamath is a cost-reduced version of Pentium Pro intended to bring that level of performance to mainstream PCs in 1997.

Although based on the P6 core used in Pentium Pro, Klamath will add the MMX multimedia extensions *(see* **100301.PDF***)*. Sources indicate that Klamath will also gain enhancements to improve performance on 16-bit code, speeding Windows 95. Such enhancements might include a segment-descriptor cache *(see* **091001.PDF***)*, a Pentium feature omitted from Pentium Pro.

We believe Klamath will be a single-chip device, breaking out of the two-chip package used by Pentium Pro. This design will give OEMs the flexibility to build systems with a greater variety of external cache sizes and speeds than Intel might want to provide. To avoid a significant performance loss, Klamath will probably include larger primary caches, perhaps as big as 32K each (four times the current size but only twice the size of the P55C's caches), along with an interface to special high-speed external SRAMs. Such a design would probably deliver nearly the same PC performance as a Pentium Pro at equivalent clock speeds.

We expect Klamath to reach clock speeds of 233 and perhaps 266 MHz using Intel's 0.28-micron CMOS version of its P854 process *(see* **090905.PDF***)*. This would be slightly faster than the 0.35-micron BiCMOS version of the Pentium Pro, allowing Klamath to outperform Pentium Pro but at a lower cost. The first Klamath products should appear early in 1997.

Intel prefers to launch a new product in a known process, in this case P854, then use that proven design to bring up a new process. By designing Klamath in pure CMOS, Intel is paving the way for a quick shrink to its forthcoming 0.25-micron process, which does not support BiCMOS. This 0.25-micron part, according to our guides, is called Deschutes. In the real world, specifically Oregon, the Deschutes River flows north into the Columbia, splitting the state in half.

Because the 0.28-micron version of P854 uses the same metal pitches as the 0.35-micron version, the Klamath die will be a bit larger than the 196-mm^2 Pentium Pro CPU. The 0.25-micron process, however, will have smaller metal pitches and perhaps a fifth metal layer, bringing the die size of Deschutes down to around 120 mm^2, enough to allow high-volume, low-cost production.

The smaller transistors and shorter metal traces will boost Deschutes' clock speed to 300 and probably 333 MHz by 2H97. It will therefore debut at premium price points, but the processor's low cost structure will allow it to become Intel's volume product in 1998 and 1999. The smaller transistors will also allow Deschutes, probably in a low-voltage version, to succeed P55C in high-end notebooks.

The successor to Deschutes, we believe, is a muscle-bound P6 (Rogue? Umpqua? Willamette?) that we know only as the P68. We speculate this device will expand the instruction-decoding capabilities and reorder buffer of the P6 core, perhaps even adding a function unit, but will retain the basic pipeline and overall architecture of the P6, reducing design and verification time. Even with relatively minor changes, a design like this could outperform Klamath by 50% or so on a per-clock basis, albeit with a much larger die. We expect the P68 to debut in late 1997 and hold the high end throughout 1998.

Our river tour ends on the Merced, which flows from California's Yosemite National Park directly toward Intel's blue headquarters complex in Santa Clara, although it stops halfway in the San Joaquin Valley. Intel's Merced will be the first chip to implement the 64-bit architecture jointly developed with HP *(see* **1001MSB.PDF***)* and, if all goes well, should appear in late 1998. The project formerly known as P7 has occasionally been referred to as Tahoe (a lake on the California-Nevada border), but that code name is more properly applied to the whole Intel-HP relationship.

While Intel's Santa Clara team works on Merced and its Hillsboro architects focus on the P68, HP is said to be developing what would have been called the P8 under the old nomenclature. (No word on its river name.) By adding HP's resources to its two main design teams, Intel will bring to market an unprecedented number of new cores in 1997 and beyond. With Intel's key competitors only now bringing their Pentium-class chips to market, they will have to double their efforts to keep pace with Intel's aggressive 1997 plans. MPR