IBM Pushes PowerPC 604 to 180 MHz

In a surprise move, IBM Microelectronics announced volume shipments of PowerPC 604 processors at 166 and 180 MHz using the same design as its 133- and 150-MHz parts. A company spokesperson indicated that the part is seeing much better speed yields than expected, allowing IBM to ship the faster parts without any circuit modifications or significant changes to the 0.44-micron CMOS-5S process.

At 180 MHz, the 604 is estimated to deliver 5.8 SPECint95 and 5.0 SPECfp95 (base) in a system with a 1M cache, 60-MHz bus, and SDRAM memory using current compilers. IBM did not, however, release any SPEC95 scores measured on a commercially available system.

The first systems to use the faster 604 come from Power Computing (Austin, Texas). With a 512K cache, 16M of DRAM, a 2G disk, and a 4× CD-ROM, the 180-MHz Power Tower lists for $4,195. Compared with the aggressive configuration quoted above, this unit would score about 10% lower on SPECint95 and 30% lower on SPECfp95 if it could run the SPEC suite, but the Mac OS–based system cannot.

In quantities of 1,000, IBM is selling the 604-180 for $693 and the 604-166 for $499. These prices match the two parts against the Pentium Pro at 200 and 150 MHz, respectively (see below), but the Pro delivers better performance on integer and floating-point tests and includes 256K of cache. Thus, the new 604s do little to advance PowerPC's position against Intel, but they do extend the family's high end, filling the gap until the 604e appears in the next few months.

Motorola did not match IBM's faster 604 parts; it still has not announced a 604-150. The company is, however, forging ahead with a version of the PowerPC 620 code-named Red October. As we predicted long ago *(see* **0914MSB.PDF** *)*, the 620 has been recast in a 0.35-micron process to improve performance and reduce cost. Sources indicate the part is now sampling at speeds as high as 200 MHz, although Motorola would not commit to volume shipments at that speed. Final production is slated for 2H96.

Pentium Pro Prices Approach $500

With its latest round of price cuts *(see* **1006CW.PDF** *)*, Intel has brought the price of Pentium Pro processors as low as $534, a 34% cut from the previous quarter. Although this price is good only for the 150-MHz version, even the speedy 200-MHz Pentium Pro, with 256K of L2 cache, now costs just $707. These price cuts are supported by better-than-expected yields on Intel's 0.35-micron lines, giving it enough capacity to pump out plenty of Pentium Pros without hampering its Pentium production.

The 150-MHz Pentium Pro now sits just above the top of the Pentium line, currently a 166-MHz Pentium listing for $498. Most of the Pentium chips received the now-standard 20–25% price cut this quarter. The biggest action happened at the low end, where the Pentium-100 now sits at $134, a 33% cut from last quarter and now less than half its price of just six months ago. As in 1Q96, the Pentium-90 carries the same price as the Pentium-100, and the Pentium-75 remains at the low-end price point of $106. These two chips are rapidly disappearing from the desktop PC market due to the small price premium for the 100-MHz version.

Intel plans to draw 90% of its processor shipments from its more efficient 0.35-micron lines by the end of this year. As a result, the older 0.5-micron parts (120 MHz and below) are being shifted to lower price points. By the end of the year, we expect the 75- and 90-MHz Pentiums will disappear entirely from Intel's price list while the 100- and 120-MHz versions reach the very low end. For Pentium Pro, we expect the 0.5-micron 150-MHz version will be phased out in 2H96 in favor of the faster 0.35-micron parts.

Intel to Sell Klamath Daughtercards

Sources indicate that Intel will offer its P6-based Klamath processor on a daughtercard with cache memory. Klamath is similar to the current Pentium Pro CPU but will be housed in a single-chip package with a separate bus to the second-level cache. The daughtercard design allows this new bus to be contained within the card; only the main system bus, presumably the same as used by Pentium Pro, will be carried through the connector to the motherboard. Intel would not discuss whether it will also sell Klamath chips individually or whether the daughtercards will come complete with SRAM or with empty SRAM sockets.

Establishing a consistent processor card for various clock speeds of Klamath and follow-on devices would give PC makers flexibility to easily configure systems with the appropriate CPU and cache size. The design also allows Intel to use third-party SRAM in standard packaging rather than building or buying bare die, as it does for Pentium Pro today. The daughtercard will, however, obsolete the current Pentium Pro form factor; Intel is unlikely to continue to support this low-volume form factor in addition to the high-volume Klamath daughtercard.

At WinHEC, Intel's Mike Aymar dropped the first official hints about Klamath. He didn't use that code name, however, referring instead to a "P6-family processor with MMX technology" expected to ship in 1H97. This terminology suggests that Intel won't market Klamath under the name Pentium Pro, at least not for home users.

Aymar also disclosed for the first time Intel's target for P55C performance. The forthcoming processor includes unspecified pipeline enhancements that increase performance compared with a standard (P54C) Pentium at the same clock speed. Aymar said the P55C will deliver a 15% improvement on typical (non-MMX) PC applications, a significant jump. By this measure, a P55C-150 should outrun a

Pentium-166, and a P55C-166 should beat a Pentium-200. With both P55C and Klamath sporting the new MMX instruction set, non-MMX processors will be completely expunged from Intel's lineup by the end of 1997, according to the vendor.

New MicroSparc CPU Has PCI Interface

Sun Microelectronics has produced its first new embedded SPARC chip in more than two years. The MicroSparc-2ep is a full-featured 100-MHz implementation of the eponymous desktop processor *(see* **071501.PDF** *)*. Instead of the SBus controller used by the workstation version, however, the 2ep has a PCI interface, a first for SPARC chips. This change allows designers to choose from the wide range of low-cost PC and embedded peripheral chips that use the PCI bus; Sun offers an SBus-to-PCI chip that gives the same options to its other processors, but the new device eliminates the need for this bus bridge.

The 2ep includes the same CPU, FPU, 16K/8K instruction/data caches, and 64-bit memory controller as MicroSparc-2. This combination of FPU, PCI, 64-bit memory interface, and high clock rate pushes it into the upper reaches of the embedded performance spectrum. It is rated at 3 W (typical), significantly less than the workstation version. We believe the chip will be built in a 0.35-micron process to reduce cost and power, but Sun would not confirm this.

The 2ep is expected to sample in 4Q96, with production slated for early 1997. Pricing for the 2ep, which comes in a 256-contact plastic BGA, has not been set, but Sun is aiming for less than $100 in "high volume." MicroSparc-2, in contrast, sells for well over $400. Sun is targeting networking boxes (naturally) with its new processor.

Philips Doubles Up on PDA Processors

Following shortly behind its so-called OneChip PDA, Philips has announced a new microprocessor that might be dubbed a "One-Chip FeaturePhone." The new chip is faster and more capable than its predecessor, and it is aimed at makers of high-end telephones, Internet terminals, and wireless PDAs.

The PR31100, like the 30100 *(see* **1001MSB.PDF** *)*, is based on an R3000-series MIPS core. The 31100 upgrades the instruction cache to 4K and doubles the clock speed to 40 MHz. More important, the new chip includes a hardware MAC (multiply-accumulate) unit, which will greatly accelerate pseudo-DSP functions like echo cancellation and telecom codecs. In fact, Philips is bundling the chip with code for a software fax/modem, which it developed internally.

A mixed-signal sidekick, called the UCB1100, acts as an analog companion to the 31100. The smaller chip's ADC can monitor a touchscreen and battery levels while its codecs massage telephone-line and audio interfaces. With Philips' software, the pair of chips can synthesize a V.32 or V.32 terbo modem up to 19.2 kbps and V.29 fax at 9,600 bps.

Both chips are now sampling, with production scheduled for 3Q96. Philips is quoting only 100,000-piece pricing for the two chips and the fax/modem software together: $38. At that price, the PR31100/UCB1100 makes an attractive package for OEMs intent on investigating the market for low-end PDAs or high-end telephones.

Tredennick Named IEEE Fellow

We'd like to offer our congratulations to long-time *Microprocessor Report* contributing editor Nick Tredennick, who was recently named an IEEE Fellow for his accomplishments in microprocessor design. Nick was a key member of the pioneering 68000 design team at Motorola and has since spent time at NexGen and Altera. He is currently an independent consultant.

S-MOS 3D Chip Leverages Frame Buffer

Attacking the huge PC installed base, S-MOS Systems' (San Jose, Calif.) new 3D graphics accelerator will bring the cost of building a complete 3D-graphics add-in card as low as $60. The SPC1515 is a single chip that does not have its own local frame buffer. Instead, it shares the frame buffer with the existing 2D graphics in the system and renders pixels over the PCI bus. In addition, the 1515 stores its texture memory in the PC's main memory. Therefore, a 1515-based add-in card consists of only a single chip and a PCI connector.

The 3D rendering architecture of the 1515 was developed by startup Reality Simulation Systems (San Jose, Calif.), with which S-MOS recently established a long-term joint development and marketing agreement for the design of 3D products for the PC market. Under the agreement, S-MOS will supply all manufacturing (through corporate affiliate Seiko Epson), worldwide sales and marketing, and codevelopment resources for Reality's designs.

The 1515 includes most common 3D features, such as Gouraud shading, perspective correction, Z-buffering, double buffering, per-pixel fog, and depth cueing. It even handles polygon setup, which today exists in only a few 3D accelerators such as the 3Dfx Voodoo and Rendition's Verite *(see* **100601.PDF** *)*. The 1515 architecture is also unusually scalable: it allows multiple 1515 chips to coexist in a system to improve performance. This expandability has been found only in architectures like VideoLogic's PowerVR.

On the other hand, the 1515 supports only point-sampled texture mapping, which is below today's standard; most current 3D products provide at least bilinear filtered texture mapping. In addition, it is questionable whether the 1515 can provide balanced 3D performance. S-MOS claims the chip can render 66 million pixels per second, but such figures are often misleading.

In reality, the 3D performance of 1515-based add-in cards will be very system dependent. These cards may work well in systems that have plenty of main-memory and frame-buffer capacity as well as PCI bandwidth to spare. An 8M sys-

tem running Windows 95, however, does not have space for a sizable texture memory. Most 2D graphics cards have only 1M or less for their frame buffers, hardly enough for 3D applications. In addition, the frame-buffer datapath efficiency can limit how fast the 1515 can render pixels. In short, the 1515 is an ultra-low-cost 3D solution, but its performance will vary widely across system configurations.

The 1515 is packaged in a 208-pin PQFP and sells for $55 in quantities of 10,000. Production is scheduled for 3Q96. We believe this chip will do well in the add-in market because of its low cost, although many end users may be disappointed with the actual delivered performance. In the long run, the growth in 3D will be for motherboard-based chips; S-MOS will need a different product to address this need.

MoSys Turns DRAM into Cache Memory

Alternative DRAM vendor MoSys (San Jose, Calif.) has reconfigured its fast DRAM core as a pin-compatible replacement for the SRAMs used in L2 caches. The MCache chip is organized as 32K×32 and provides 3-1-1-1 operation at 66 MHz or 75 MHz. This is the same performance as pipeline-burst (PB) SRAM but with one-third the die size and one-third the active power consumption. These savings come from the use of single-transistor DRAM memory cells instead of the traditional four-transistor SRAM cell.

The downside of DRAM storage is that it must be refreshed, so system-logic chip sets must be redesigned to refresh the MCache. Intel's 430HX and 430VX *(see* **1002MSB.PDF** *)* as well as VIA's Apollo VP chip set include the necessary logic to support MCache. These refresh cycles impose a performance penalty of "well under 0.5%," according to MoSys.

Four signal pins, defined as no-connects in PB SRAM chips, support the unique MCache operating features. These include HW/R#, RESET#, and two proprietary "function" pins. Intel's COASt (cache on a stick) specification already directs OEMs to connect these signals to the cache controller, so existing motherboards with 430HX, 430VX, and Apollo VP chip sets should work correctly with MCache-based cache modules. The operation of the proprietary pins, however, still has not been revealed.

Power consumption is low—less than 300 mW (peak) at full speed, compared with 1 W for PB SRAM. Standby power is also very low, less than 1 mA, making the new device well suited for portable systems.

IDT, which holds an equity interest in MoSys, will manufacture the device; both MoSys and IDT will sell it. The first part, the IDT71F432, will be made on IDT's 0.5-micron process and will be available in production quantities in May. The 71F432 is sold in a 100-pin TQFP package and in 256K DIMM modules for Pentium motherboards. MoSys will sell the device as the MC80132K32Q in a 100-pin PQFP package and in module form as well. Pricing is estimated at $7.50 in thousands, roughly the same as PB SRAM; we expect MCache pricing will drop below SRAM by year's end.

The potential market for these devices is quite large; we project 55 million Pentium-class microprocessors will be sold this year, and most will be matched with two or more SRAMs. MoSys intends to aggressively pursue this market, taking advantage of its bit-density advantage to build larger devices at the same price as current SRAM chips.

Silicon Magic Launches Fastest EDO

Startup Silicon Magic (Cupertino, Calif.) today announced its first extended data out (EDO) DRAM with access times of 35 ns. At 66 MHz, the device offers the best available performance in a 4-Mbit configuration for desktop graphics applications, digital signal processing, networking, and other high-end computing systems. The part leverages the advanced technology of Silicon Magic's earlier 60-MHz EDO DRAM.

The SM81C256K16A1-35 is a 256K×16 device with random access times down to 35 ns; in EDO cycle operation, column accesses occur every 15 ns. The product uses a single 5-V power supply and offers three refresh modes: RAS only, CAS-before-RAS, and hidden.

The product is shipping now in 40-pin SOJ packages and is priced at $12 each in production volumes. Because of its fast access time, the 35-ns device can provide much higher data bandwidth than today's typical 60-ns EDO, and this bandwidth is critical for multimedia applications, especially 3D graphics. This part should generate great interest from companies such as Rendition and S3.

LSI Logic MPEG Encoder Programmable in C

LSI Logic has rolled out a new chip set for real-time encoding of audio and video. All three chips in the set are based on LSI's CW4001 MIPS core *(see* **081703.PDF** *)* combined with different compression, filtering, and scanning functions. Taking a hint from Sun, LSI has labeled the family VISC, for visual instruction-set computing, and touts the fact that the entire chip set can be programmed in C or C++.

The VISC set can encode audio and video according to MPEG-1, MPEG-2, DigiCipher, or H.261 standards. The number of chips required depends on the encoding method and the desired quality. For example, MPEG-1 encoding requires only two chips, while MPEG-2 requires five. Each chip is autonomous and requires its own frame buffer; partially compressed images and control information are passed over a shared bus.

The market for real-time encoding is still relatively small but growing rapidly as digital satellite broadcasting and multimedia authoring increases. By offering high-level language tools for its chip set, LSI hopes to woo developers unfamiliar with the ins and outs of audio and video encoding algorithms as well as those who, with markets and standards still shifting, value quick development time. M