# PATENT WATCH

*by Rich Belgard, Contributing Editor*

*The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to* belgard@umunhum.stanford.edu

## 5,479,616

*Exception handling for prefetched instruction bytes using valid bits to identify instructions that will cause an exception*
Issued: December 26, 1995
Inventors: Raul A. Garibay, Jr., et al
Assignee: Cyrix
Filed: April 3, 1992
Claims: 11
A 486-type microprocessor includes a prefetch unit that appends a valid bit to each prefetched instruction byte as it stores it into a prefetch queue. This valid bit notifies the instruction decoder if the byte is not valid (such as resulting from a branch). If the prefetch unit detects that any of a selected number of exception conditions (such as limit violations and page faults) apply to a prefetched instruction byte, it also clears the valid bit. An exception processor is invoked as a result of a cleared valid bit.

## 5,477,488

*System, a memory, and a process having bit-processing circuits associated with memory for preprocessing data read by a processor*
Issued: December 19, 1995
Inventor: K. Subramani
Assignee: Texas Instruments
Filed: February 14, 1994
Claims: 8
Bit-processing circuits on the substrate of memory circuits perform bit operations on the data before producing the processed data from the memory. A system includes a CPU on a separate substrate that produces bit-operation information in a time-multiplexed sequence on the address leads or to normally not-connected leads on the memory substrate.

## 5,475,824

*Microprocessor with apparatus for parallel execution of instructions*
Issued: December 12, 1995
Inventors: Edward T. Grochowski
Assignee: Intel
Filed: February 10, 1995
Claims: 14
A computer system includes a dual instruction decoder that issues two instructions in parallel within a single clock cycle if there are no register dependencies between the instructions and the instructions fall within a predetermined subset of the complete instruction set. The system includes two pipelines. The first pipeline executes any instruction issued from the full instruction set, while the second pipeline executes only a subset of instructions. A register dependency checker checks for dependencies. When both instructions are in the subset and there are no register dependencies, the two instructions are issued to the two pipelines in parallel.

## 5,473,575

*Integrated circuit I/O using a high-performance bus interface*
Issued: December 5, 1995
Inventors: Michael Farmwald, et al
Assignee: Rambus
Filed: March 5, 1992
Claims: 6
The invention includes a memory subsystem of least two chips, including at least one memory device, connected to a bus, where the bus carries address, data, and control information needed by the memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address. Furthermore, the bus carries device-select information without the need for separate device-select lines connected directly to individual devices. The invention also includes master/slave protocol for the bus.

## OTHER ISSUED PATENTS

**5,475,853** *Cache store of instruction pairs with tags to indicate parallel execution*
**5,479,622** *Single-cycle dispatch delay in a multiple-instruction dispatch mechanism of a data-processing system*
**5,479,639** *Computer system with a paged non-volatile memory*
**5,475,856** *Dynamic multimode parallel processing array*
**5,475,829** *Computer system which overrides write protection status during execution in system-management mode*
**5,475,828** *Digital processor having plurality of memories and plurality of arithmetic logic units corresponding in number thereto and method for controlling the same*
**5,475,823** *Memory processor that prevents errors when load instructions are moved in the execution sequence*
**5,475,822** *Data-processing system for resuming instruction execution after an interrupt and method therefor*
**5,475,630** *Method and apparatus for performing prescaled division*
**5,475,565** *Power-distribution lid for IC package*
**5,473,774** *Method for conflict detection in parallel-processing system*
**5,473,767** *Method and apparatus for asynchronously stopping the clock in a processor*
**5,473,763** *Interrupt vector method and apparatus*
**5,473,572** *Power-saving system for a memory controller* M