PowerPC Team Outlines Future Plans

Multiple Projects in Progress; Likely to Keep Pace with Intel

by Linley Gwennap

Now that the PowerPC vendors have nearly completed their original 1991 processor roadmap, they have begun to discuss the products that will extend the current line into the future. IBM and Motorola unveiled a new roadmap that includes three major efforts, all of which are simultaneously under development at the Somerset Design Center.

Next year will see the debut of parts code-named G3, derivatives of the current 603e and 604e but with bigger caches and improved system interfaces. Although derived from the current parts, they will probably have new names. The G4 parts, due in 1998, will include a new PowerPC CPU core. Somerset has also begun development on Project 2K, which may implement a radically new design.

The PowerPC vendors, of course, claim these parts will establish a significant performance lead over Intel's offerings at any given price point over time. Neither the PowerPC team nor Intel has offered enough information on these future products to evaluate these claims. Unless Intel has a major stumble, however, there is nothing in the PowerPC roadmap to indicate a significant performance advantage.

Changes at Somerset

The PowerPC alliance has been through some trying times *(see* **100101.PDF***)*. The initial versions of the 604 and 620 were buggy and delivered disappointing performance. The effort needed to fix these problems delayed work on new products. Neither IBM nor Motorola was able to match Intel's IC process capabilities at that time. In the meantime, conflicts caused by joint IBM and Motorola management of Somerset led many engineers to quit in disgust.

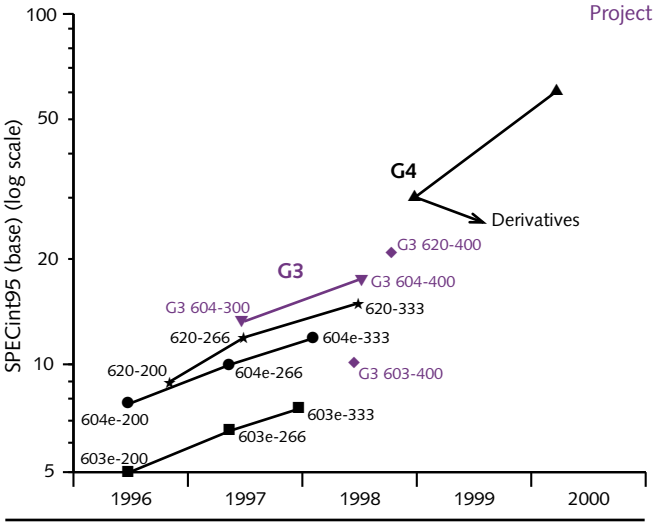

Figure 1. Our forecast of PowerPC processors, based on the new roadmap, shows a plethora of parts. (Source: MDR, Somerset)

The partners have not given up on their ambitious goals of being leading players in the PC market and instead have intensified their efforts. The staff at Somerset has been increased by 50% over the past year to accelerate work on multiple generations of PowerPC processors. Perhaps more important is the reorganization that eliminated the two-headed management structure. Somerset is now managed solely by Mark McDermott, and each project team is also led by one manager, not two.

IBM and Motorola have made massive investments to improve their IC process technology over the past two years. The mainstream PowerPC processors are now built in 0.35-micron CMOS *(see* **100703.PDF***)*, similar to Intel's current products. The partners plan to move to a 0.25-micron process by 2H97, only a few months behind Intel's planned conversion. The partners have a goal of delivering products at below 0.1 microns by 2001, which would put them well ahead of Intel, but this goal is so far ahead of the rest of the industry that it seems unattainable, particularly since the steppers and other equipment needed for 0.1-micron fabrication will simply not be available. At best, continued aggressive investment should let the PowerPC vendors keep pace with or even pull slightly ahead of Intel.

Despite these changes, the poor execution at Somerset will continue to impact the PowerPC alliance for some time. The 603 and 604 processor cores, which were essentially complete in 1994, must drive the PowerPC line until late 1998, when the first G4 parts appear. Even with the G3 enhancements, without a new core there is little opportunity for PowerPC to gain a significant performance advantage over Intel's P6 family during this period.

Enhancements to Current Parts

As Figure 1 shows, the 603e and 604e, which include twice the cache of the original 603 and 604, will continue to be upgraded throughout 1997. In addition, the 620, which should begin shipping late this year, will also be improved. The companies expect to move all the parts to new IC processes at about the same time, although the 620 may lag a bit. Since the parts use similar pipeline designs, they are likely to run at about the same clock speeds in the same IC process.

In 1H97, the three PowerPC processors are slated to move to 0.29-micron CMOS, which we believe will push clock speeds to about 266 MHz. This move should also provide a significant decrease in die size and thus manufacturing cost. By 2H97, a gate shrink to 0.25-micron CMOS could put the parts at 333 MHz or so.

Third Generation Adds to Current Cores

During 1997, the first G3 parts will appear. (G3 indicates third generation; the 601 counts as the first generation, while the current parts represent the second.) Somerset is already testing first silicon of the initial G3 design, which suggests first system shipments by mid-1997. The vendors would not discuss the specifics of these parts but said they will combine the current CPU cores with larger on-chip caches, separate L2 cache buses, and possibly a new system bus.

As the current cores exceed 200 MHz, the limited bandwidth of the 60x system interface, similar to that of Pentium, becomes a serious performance bottleneck. Increasing the core CPU clock speed to 300 MHz and beyond will improve performance, but the system interface must be changed to keep pace. Adding a separate high-bandwidth L2 cache bus to the 604 would ease the bandwidth pressure on the system bus. Adding a split-transaction system bus would improve main-memory performance and simplify multiprocessor systems. The G3 604 is likely to look very much like a 32-bit 620, although probably with larger on-chip caches.

A larger on-chip cache would reduce the bandwidth requirement for the L2 cache and could even make the L2 cache optional in low-cost systems. The PowerPC roadmap shows G3 processors with up to 30 million transistors. One possibility is a 603 core combined with 256K or 512K of on-chip cache and no external cache. This design could be built in 0.25-micron CMOS and would provide good performance. The integration would provide footprint and power savings for portable systems. IBM's redundancy techniques should allow high yields in these SRAM-dominated parts.

The 620 already has a separate L2 cache bus and enhanced system interface, so the only enhancements likely in the G3 generation are larger caches. The 620's caches could be enlarged to 64K each, or even 128K each, as the chip is shrunk to 0.25-micron CMOS.

The vendors indicated they may make some minor improvements in the CPU cores themselves, including circuit tuning that would push clock speeds as high as 400 MHz. These enhancements will not, however, include new multimedia instructions to match Intel's MMX.

A New Core for G4

The G4 family will include a new PowerPC core. The companies would say little about the G4 core other than that it will use "advanced design methods" and that it will match the native-mode performance of the Intel/HP Merced processor. (That several RISC vendors are now comparing the performance of their next-generation processors to Merced reflects the new role Intel has taken in the high-performance arena.) Both Merced and the G4 are expected around 2H98.

We expect the G4 to continue on the path of increased dispatch width, more function units, and added reservation stations to increase the window for out-of-order execution. It appears the G4 will debut in a 0.25-micron process at about 400 MHz, with a future 0.18-micron version exceeding 500 MHz. These speeds seem fast, but given that Digital is achieving 500 MHz from a 0.35-micron process today, they are relatively modest. Somerset appears unwilling to push too hard on clock speed, the most direct leverage point for CPU core performance. IBM's design methods and tools are notoriously conservative in this regard, which may prevent the chips from achieving performance leadership.

An advanced memory hierarchy is needed to service the demands of such a high-performance processor. The roadmap indicates a transistor count of "up to 50 million," which implies a complex processor with 512K or so of on-chip cache, perhaps divided into two levels.The G4 will leverage the system interface (advanced system bus and separate external cache bus) of the G3 604, simplifying system designs and accelerating its adoption. The G3 parts are likely to continue to service the bulk of PowerPC volume in 1999 as the G4 proliferates into multiple versions and comes down in price.

The G4 core will be Somerset's next opportunity to introduce instruction-set extensions to PowerPC. The vendors would not commit to multimedia extensions in G4, however, and more exotic instructions are unlikely. The partners seem to be holding off on such changes until Project 2K, which is not due until 2000 or 2001.

A Clean Sheet of Paper

A small team at Somerset is working on the architecture for Project 2K. Like the Merced team, the 2K designers have been allowed to start from scratch and (like the Merced team) are likely to produce a new instruction set with more registers, more "hints" from the compiler to the hardware, and other enhancements *(see* **101003.PDF***)*. Properly designed, the 2K processor should be able to provide compatibility with PowerPC binaries without extensive hardware overhead. This is one area where PowerPC has an advantage over Merced; emulating x86 binaries will be more difficult, although quite possible.

In general, however, Project 2K appears much like the Intel/HP effort, but two or three years later. Somerset claims this lag will give it time to produce a better design than Merced, and there may be some small advantage in waiting. But the biggest effect is that Intel will have a significant head-start in convincing software vendors to support its new instruction set, and that is the critical factor.

The combined efforts behind the G3, G4, and 2K products are immense and establish PowerPC as a steadfast contender in the PC processor market. We expect these efforts will keep PowerPC on par with Intel's performance over the next few years. Manufacturing-cost advantages and aggressive pricing should allow PowerPC processors to maintain a price/performance advantage over Intel's at the chip level. But unless the lineup of PowerPC system vendors changes significantly, these price/performance advantages will not be visible at the system level. Thus, Macintosh users will be happy, but nothing in the new roadmap indicates an advantage that will cause x86 users to switch to PowerPC. M