PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,497,499

Superscalar RISC instruction scheduling
Issued: March 5, 1996
Inventors: Sanjiv Garg, et al
Assignee: Seiko Epson
Filed: March 29, 1994
Claims: 16
A register-renaming system for out-of-order execution of RISC instructions having addressable source and destination register fields. A data-dependence check circuit is included for determining data dependencies between the instructions. A tag-assignment circuit generates one or more tags to specify the location of operands, based on the data dependencies determined by the data-dependence check circuit. A set of register-file port multiplexers selects the tags generated by the tag-assignment circuit and passes the tags onto the read-address ports of the register file for storing execution results.

5,497,496

Superscalar processor controlling fetching of instructions based upon number of empty instructions registers detected for each cycle
Issued: March 5, 1996
Inventor: Hideki Ando
Assignee: Mitsubishi
Filed: July 28, 1994
Claims: 12
Multiple instructions are read out of an instruction cache each cycle, temporarily stored in a shift register, then transferred to empty positions of four instruction registers. An instruction decoder selects instructions that can be processed in parallel from the four instruction registers and supplies them to any of four processing units. A selector-control circuit controls selectors based on a signal indicating the number of empty instruction registers.

5,497,477

System and method for replacing a data entry in a cache memory
Issued: March 5, 1996
Inventor: Jeffrey E. Trull
Assignee: None
Filed: March 7, 1994
Claims: 13
A cache-insertion selector for selecting a slot of a memory cache in which to insert data is described. The access history of a slot is monitored with a single boolean variable called "used recently." A slot is marked as "used recently" when it is accessed. When a new entry is to be inserted, the cache-insertion selector attempts to select a slot that is not marked as "used recently." If all slots are marked as "used recently," the cache-insertion selector marks all slots as "not used recently" and selects one slot.

5,497,472

Cache-control method and apparatus for storing data in a cache memory and for indicating completion of a write request, irrespective of whether a record to be accessed exists in an external storage unit
Issued: March 5, 1996
Inventors: Akira Yamamoto, et al
Assignee: Hitachi
Claims: 20
Filed: January 19, 1995
A computer with a CPU, a control unit for a cache, and a storage unit is described. If the control unit receives a write request for data to be written and the data to be written is not being stored in the cache, the control unit receives the data and stores it in the cache memory. The cache unit notifies the CPU of a completion of a data write, then checks if the data is being stored in the storage unit. If so, the data in the cache is written into the storage unit; if not, the data in the cache is not written and remains in the cache.

5,497,344

Data-flow-type information processor
Issued: March 5, 1996
Inventor: Toshiya Okamoto
Assignee: Sharp
Filed: July 15, 1994
Claims: 7
A data packet including a destination field, an instruction field, and two data fields is output from a data-pair-detecting portion of a data-flow processor. The data packet is then divided into two packets. One packet, including the destination field and an identification tag, is sent to a program-storing portion, and another packet, including the instruction field, the two data fields, and the identification tag, is sent to an operation-processing portion. The program-storing portion outputs a packet including the destination field, the instruction field, and the identification tag. The operation-processing portion produces a packet including the result data and the identification tag. These packets are merged with each other, based on the identification tags, and sent to the data-pair-detecting portion.

OTHER ISSUED PATENTS

5,497,493 *High-byte right-shift apparatus with a register alias* M