PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,522,064

Data-processing apparatus for dynamically setting timings in a dynamic memory system
Issued: May 28, 1996
Inventors: Alfredo Aldereguia, et al
Assignee: IBM
Filed: October 1, 1990
Claims: 11
A memory controller controls access to a memory consisting of multiple modules, each of which can operate with different signal-timing characteristics. Within the controller, timing-control registers that correspond to the respective modules allow for the programming of different timing characteristics for each module. Circuitry on the controller uses the incoming memory addresses to select the timing register for the corresponding memory module.

5,522,051

Method and apparatus for stack manipulation in a pipelined processor
Issued: May 28, 1996
Inventor: Harshvardham P. Sharangpani
Assignee: Intel
Filed: September 14, 1994
Claims: 30
A pointer-register file contains a set of pointers used to map stack-relative addresses to physical register-file addresses. Both files are multiported to allow access to multiple stack entries in the same cycle. Pipeline stalls are mitigated in situations in which conventional stalls would occur.

5,519,841

Multi-instruction register mapper
Issued: May 21, 1996
Inventors: David J. Sager, et al
Assignee: Digital
Filed: November 12, 1992
Claims: 18
A register-file mechanism for use in a pipelined superscalar processor that includes a logical register-file remapper and multiple register files is disclosed. The remapper renames instruction operands of simultaneously issued instructions onto the register files such that each instruction is assigned to its own register file.

5,517,651

Method and apparatus for loading a segment register in a microprocessor capable of operating in multiple modes
Issued: May 14, 1996
Inventors: Kamla Huck, et al
Assignee: Intel
Filed: December 29, 1993
Claims: 39
A generalized series of steps for loading a segment register in an x86 microprocessor that can operate in multiple modes. A microcode routine and logic for processing a segment-register load are described.

5,515,521

Circuit and method for reducing delays associated with contention interference between code fetches and operand accesses of a microprocessor
Issued: May 7, 1996
Inventors: Graham Whitted III, et al
Assignee: Meridian Semiconductor
Filed: February 8, 1994
Claims: 28
An access-control unit for a microprocessor receives fetch requests and operand-access requests from a CPU of the microprocessor and issues the requests to a bus/cache unit in a manner that reduces interference between fetch requests and operand-access requests.

5,515,518

Two-level branch-prediction cache
Issued: May 7, 1996
Inventors: David R. Stiles, et al
Assignee: NexGen
Filed: July 5, 1994
Claims: 31
A branch-prediction cache uses a two-level scheme. The first-level cache contains a relatively small number of entries containing full branch-prediction information. The second-level cache contains a larger number of entries containing less branch-prediction information. It the branch data exists in the first-level cache, it is used. If not, then the second-level cache is used.

OTHER ISSUED PATENTS

5,522,057 *Hybrid write-back/write-through cache having a streamlined four-state cache-coherency protocol for uniprocessor computer systems*
5,519,864 *Method and apparatus for scheduling the dispatch of instructions from a reservation station*
5,517,657 *Segment-register file read-and-write pipeline* M