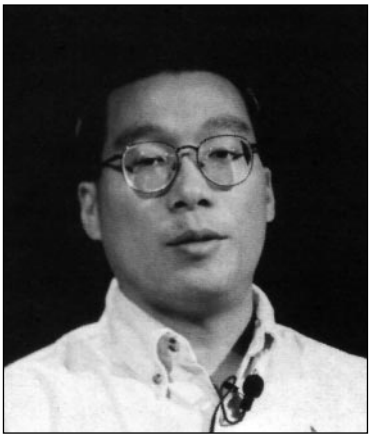
QED's PowerPC 603q Heads for Low Cost

Design Firm Wraps Its First PowerPC Chip; Future of the Part Still Uncertain

by Jim Turley

The inveterate MIPS jockeys at Quantum Effect Design have backed a second horse and developed their first PowerPC microprocessor. At last month's Microprocessor Forum, QED engineer Bryan Chin trotted out the 603q, a midrange PowerPC that delivers performance similar to the 603e's but at half the power and two-thirds the die area.

The 603q was aimed at low-end desktop and high-end embedded designs. Was, that is, until QED's unnamed customer prepared to pull the plug on the project scant weeks after it taped out. Because QED has no PowerPC license of its own, it cannot sell the chip except to a licensed fab. The company is now left with a completed PowerPC design and potentially no customer to sell it to.



MICHAEL MUSTACCHI

QED engineer Bryan Chin discusses the PowerPC 603q at the Microprocessor Forum.

The Vanishing PowerPC Client

QED recently shifted its business strategy from a design-for-hire service to that of a fabless microprocessor vendor *(see* **1012MSB.PDF***)*. The company's stated goal is to develop high-end embedded CPUs based on MIPS and "other mainstream instruction sets," implying the door is open to more PowerPC designs and perhaps even other architectures. But building and selling PowerPC chips requires a PowerPC license, a nontrivial expense that a small company like QED can ill afford at this stage.

	602	603q	603e	603e
Clock Frequency	80 MHz	160 MHz	120 MHz	240 MHz
Instr Cache Size	4K	16K	16K	16K
Data Cache Size	4K	8K	16K	16K
Power (typ)	1.45 W	1.6 W	3.5 W	4.5 W
Dispatch (sustained)	1 instr	1 instr	2 instr	2 instr
Dispatch (peak)	2 instr	1 instr	3 instr	3 instr
FP Repeat Rate, DP	n/a	4 cycles	2 cycles	2 cycles
FP Repeat Rate, SP	1 cycle	4 cycles	1 cycle	1 cycle
External Bus I/F	Mux'd	Mux'd	Demux'd	Demux'd
IC Process	0.5µ 4M	0.5µ 3M	0.5µ 4M	0.35µ 4M
Die Size	50 mm²	69 mm²	98 mm²	79 mm²
List Price (1,000s)	$37	n/a	$121	$408
Availability	Now	n/a	Now	Now

Table 1. The 603q does not have the superscalar features of other midrange PowerPCs, but its small die size and modest power requirements make it competitive in high-end embedded systems. (n/a = not applicable) (Source: vendors)

The alternative is to design PowerPC parts solely for licensees, namely Motorola, IBM, Exponential, or Apple. The restrictive terms of Exponential's unusual license agreement might not allow it to build or sell QED's design, and Apple is unlikely to start manufacturing chips any time soon. That leaves IBM and Motorola as QED's sole potential customers, one of which appears likely to back out.

Although QED is mum, other sources suggest the client was Motorola, and ultimately Apple. The rapid pace of PowerPC speed improvements in the past several months coupled with Apple's bad experiences trying to sell low-end Macs in 1996 and the fact that both Motorola and IBM already have embedded PowerPC cores may have all conspired against the 603q.

QED's situation is not hopeless. The company owns all the intellectual property embodied in the 603q, which can be leveraged for a new, similar design. It also now has its own PowerPC verification suite, test vectors, and software.

No-Frills Design Cuts Cost, Speed

The 603q was intended for cost-effective desktop applications, moving into high-end embedded systems over time. The market targets meant that QED could afford to emphasize the integer unit over floating-point performance. The goal was not to beat existing PowerPC chips in a horse race but to provide similar performance at a more competitive price. To reach those goals, QED fell back on its strengths, developing a fast but simple pipeline and surrounding it with lots of cache.

The 603q implements a classic five-stage RISC pipeline. The part is not superscalar, nor does it implement branch prediction or independent load/store, branch, or ALU datapaths. QED's minimalist approach allowed it to squeeze the 603q onto a die just 38% larger than a 602, even though its caches are three times bigger. Table 1 outlines the differences between the 603q and its nearest competitors, the 602 and 603e.

The PowerPC integer core proved to be a true design challenge for a team weaned on MIPS microprocessors. The PowerPC instruction set is much richer than MIPS and "at the far, far end of RISC," according to QED's Chin. String operations, unaligned accesses, and multiple load/store instructions caused the biggest headaches.

Even though unaligned accesses and string operations are not part of the basic PowerPC specification, the 601

supported them, and they are used by many Macintosh applications. To achieve total Mac compatibility, the 603q had to handle these extraneous functions transparently.

According to QED's Chin, the design team was able to trade on its MIPS experience in the FP portion of the 603q, but the integer pipeline had to be developed from scratch. All IEEE 754–compatible FPUs are similar to some extent, so QED was able to reuse designs from the R4600 family. The concept of the merged integer and FP pipelines was taken from the R4650, another QED design.

The goal was to save design time and die area, but Chin said that, in retrospect, very little of either was saved, while a significant amount of FP performance was sacrificed. A more fully featured FPU, like that in the 603, might have boosted FP performance proportionally more than the extra die area it would have required.

Cache Uses Unique 6T SRAM Cell

One trick up QED's sleeve is a new SRAM-cell design. The company developed its own six-transistor SRAM cell, which it has patented. The new cell organization uses about 7–8% less die area and half the power of a conventional SRAM cell, according to the company. This same SRAM design is used for the RM7000's cache *(see* **101409.PDF***)*.

Given QED's approach to microprocessor design, it's logical the company would work on shrinking the bulkiest portion of its chips, which is the cache. As the chart in Figure 1 shows, the cache is the single largest consumer of real estate on the 603q. Since the part wasn't intended to be a performance leader, its design goals could best be met by reducing die size as much as possible. The part measures just 69 mm^2 overall.

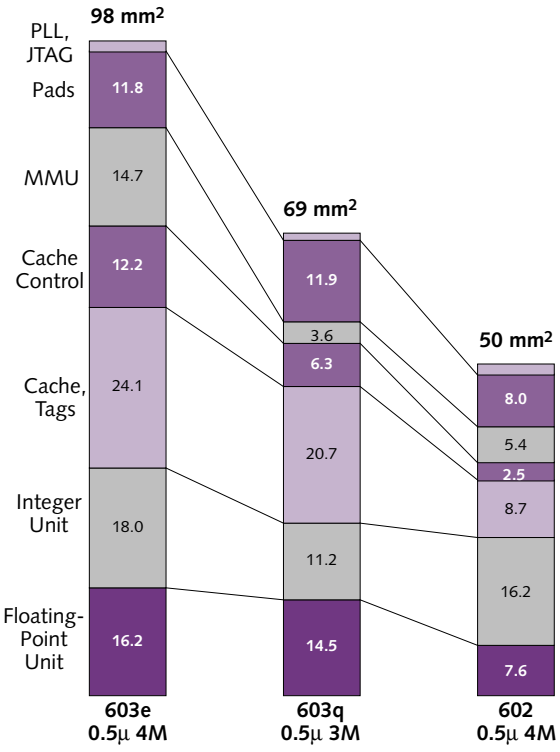


Figure 1. Comparing relative die allocation for the 602, 603q, and 603e highlights QED's ability to shrink the PowerPC integer unit by eliminating superscalar execution and branch handling. (Source: QED)

Price & Availability

Availability of the 603q is uncertain. QED may deliver derivative PowerPC devices at some point in the future. For more information, contact QED (Santa Clara, Calif.) at 408.565.0315; or visit the Web at *www.qedinc.com.*

Performance Matches Slower 603e Chips'

The 603q's bus interface is an amalgam of the 602's and 603's, with the former's multiplexed address/data bus and the latter's control-signal protocol and timing. In its CQFP-160 package, the 603q is not pin-compatible with either of those chips, although control logic or ASICs from a 603-based design could probably be reused.

QED's tests indicate the 603q achieves about 70% of the 603e's performance on the SPEC suite on a per-clock basis. The 160-MHz 603q should therefore deliver about the same integer performance as a 120-MHz 603e. FP performance will be somewhat lower due to the 603q's simplified FPU and single-issue design.

Motorola and IBM recently announced 603e parts running at 240 MHz *(see* **1014MSB.PDF***)*. These chips should deliver about twice the integer performance of the 603q, according to QED's figures, and do even better on FP. At about $400 a pop, these new PowerPCs aren't cheap; the 120-MHz 603e is much more in line with most embedded designers' budgets. Unfortunately, no pricing information is available for the 603q, nor is it ever likely to be.

What's Ahead for QED?

Certainly the company is disappointed that its first PowerPC processor may never see the light of day. The project lasted nearly two years and expanded QED's design staff significantly. Its introduction was also timed to coincide with the company's coming-out party, marking its entry into the merchant CPU business.

On the plus side, QED is willing and able to undertake a new PowerPC design armed with its new verification techniques, test vectors, and design tools. Its list of potential clients is obviously very small (i.e., two), but its record of nimble, cost-effective designs could help either IBM or Motorola win a particular customer or market segment.

In the meantime, QED will busy itself finishing its high-end RM7000 design and other MIPS processors. As its past history has shown, the company can survive quite comfortably with just one CPU architecture. M