MOST SIGNIFICANT BITS

Intel's Katmai, Willamette Surface

Intel's river map rolls onward. Rumors have recently surfaced regarding two new processors planned for 1998. Sources indicate Intel is working on a processor code-named Katmai that will be a minor improvement on Deschutes. (Katmai, pronounced KAT-mye, is named after a river in Alaska; Intel has apparently moved beyond Oregon and California in its naming conventions.)

The key to Katmai appears to be the addition of new MMX instructions, forming a set referred to as MMX 2. No word yet on what the new instructions are, but they may address 3D geometry performance, which MMX does not. One possible addition would be dual floating-point operations similar to those in MIPS V *(see* **101505.PDF***)*. Katmai is said to be planned for a 1H98 debut, about six months after Deschutes first appears.

We believe Intel is moving aggressively to improve the multimedia performance of its processors, particularly for 3D graphics, which is weak today. These moves will both drive another PC upgrade cycle and protect against a significant incursion from media processors *(see* **1013ED.PDF***)*. MMX, as originally announced, is just the first step, and subsequent Intel processors will offer continued improvement.

For the second half of 1998, Intel is preparing a much more significant upgrade, a chip code-named Willamette ("Wil-LAM-ette") after the Oregon river. This device, which we previously called the P68 *(see* **1003ED.PDF***)*, is expected to be based on the P6 core but with significant performance enhancements, perhaps including a larger reorder buffer and an additional integer unit. Willamette will presumably carry forward the MMX 2 enhancements from Katmai. As a result of these changes, we expect Willamette to deliver 30–50% better integer performance per clock cycle than Deschutes and perhaps a bigger improvement on 3D graphics and some other multimedia applications.

Intel is also said to be working on a 100-MHz version of the P6 bus, which is today limited to 66 MHz. The current speed is adequate for systems with four 200-MHz Pentium Pro processors using 512K caches and is likely to support four 300-MHz Deschutes processors if they are each coupled with around 2M of cache. A four-way Willamette server, however, will overwhelm the 66-MHz bus. Even a one- or two-CPU desktop system may need the faster bus for Willamette, since these systems will probably stick with 512K of cache. We expect Intel will support the faster bus speed as an option for Willamette, and possibly for Katmai as well.

Willamette's main role is to fill in the x86 line underneath Merced, the first IA-64 processor. We expect Willamette, along with a subsequent shrink version, will be Intel's mainstream processor throughout 1999 and 2000, giving Merced plenty of time to gain software and system support while easing into the market. —*L.G.*

New MicroUnity Chip for Cable Modems

At last month's Microprocessor Forum, MicroUnity's Craig Hansen revealed the first fruit of the company's strategic repositioning *(see* **1010MSB.PDF***)*. To replace its high-power BiCMOS chip designed for generalized signal processing, the company has developed a low-power CMOS device tuned for cable modems. The new device retains the instruction set and much of the microarchitecture of the BiCMOS chip but makes several changes to reduce power consumption.

The first change, of course, is from BiCMOS to CMOS. The original processor ran at 1 GHz; because bipolar circuits consume power whether they are switching or not, it makes sense to switch them as fast and as much as possible. This factor led to the idea of a multithreaded design that switches from one instruction stream to the next on every cycle, overlapping five threads at once.

In a CMOS process, this architecture burns far too much power: a prototype multithreaded CMOS processor was measured at 60 W despite clocking at only 200 MHz. The new chip is a traditional single-threaded design running at 113 MHz. Although the peak performance of this design is obviously greatly reduced, the throughput of a single thread is similar to that of the BiCMOS design, which ran each thread at 200 MHz but encountered greater memory latencies relative to the cycle time.

The new media processor, built in 0.35-micron four-layer-metal CMOS, runs at 3.3 V and consumes just 4 W (maximum) at 113 MHz. Although it has five million transistors, about three million are in the 64K of on-chip cache, and the die size is just 100 mm^2. It retains enough performance to handle various modulation algorithms (such as QAM, DMT, and CDMA), 802.2 bridging, and higher-level services for a cable modem.

An entire cable modem could be built from just the MicroUnity media processor and its associated media codec, 512K of DRAM, 128K of flash, a tuner for the cable input, and an Ethernet connection to the PC. The media codec provides a PCI interface, allowing the use of commodity Ethernet chips. An optional telephone modem can be added through the PCI interface as well.

By leveraging its original media processor design, the company has quickly created a new design, although prototypes have yet to be built. MicroUnity is now seeking a semiconductor partner to fabricate and market the device. With low power consumption and a small die size, the new design is much better suited to the market needs of cable modems and set-top boxes than the original BiCMOS monster. Whether the new device can save MicroUnity from extinction depends on how quickly the market for cable modems increases from its current near-zero state and whether the company has any other irons in the fire. —*L.G.*

Newton First Design Win for StrongArm

Digital's StrongArm has made its first public appearance in the form of Apple's newest Newton. As we predicted *(see* **100201.PDF***)*, the SA-110 forms the heart of the new Apple MessagePad 2000, which Apple claims runs "up to 10 times faster than any previous model" of Newton; in fact, the 162-MHz StrongArm chip is rated at 185 MIPS, compared with 18 MIPS for the ARM610 used in previous models. Other than the new CPU, the 2000 is similar to earlier Newtons. Apple expects to ship the new model in 1Q97.

The nominal 160-MHz StrongArm was chosen because its power consumption, at 1.65/3.3 V, most closely matched that of the earlier Newton's 5-V ARM610. The handheld unit is based on a commercial processor, like previous Newtons, and a set of four ASICs built by Cirrus. The 2000 also contains 8M of ROM, 4M of flash memory, and 1M of DRAM. Power is provided by four AA batteries; Apple advertises three to six weeks of useful battery life.

The new unit comes with the usual assortment of productivity applications plus a Web browser and software (with cables) for communicating with desktop Macintoshes and PCs—a notorious shortcoming of previous Newtons. Apple also claims vastly improved handwriting recognition, thanks mostly to the faster processor.

In addition to appearing in the 2000, StrongArm will be at the heart of Apple's licensed Newton reference platforms. Inexplicably, the portable eMate 300, which Apple rolled out on the same day, uses an ARM710 processor.

Digital can now trumpet its first design win for StrongArm, one that has the potential to outstrip total Alpha sales in a very short time. The company has publicly demonstrated network computers and other devices based on StrongArm, but no other customers are willing to identify themselves at this time.

Apple's decision to announce the Newton 2000 months before it is available is widely seen as a pre-emptive strike against a spate of Windows CE announcements this week. The new Newton is expected to be more expensive—perhaps by a factor of two—than the WinCE units, so Apple will again have to convince buyers that Newton's features are worth the price premium. —*J.T.*

Oak Describes Single-Chip DVD Decoder

At last month's Microprocessor Forum, Oak Technology *(www.oaktech.com)* previewed a possible future product for DVD players and similar consumer devices: a single chip combining a new 32-bit RISC processor core with multiple blocks of fixed-function logic.

The new architecture takes a different tack than other programmable multimedia processors like Chromatic's Mpact 2 *(see* **101501.PDF***)*. Instead of using a high-performance processor core to execute multimedia functions directly, the design performs the bulk of these functions in hardwired logic, relying on a fairly simple CPU core to manage the flow of data among the various logic blocks.

Hardwired functions include an MPEG-2 transport stream parser, MPEG-2 video and audio decoders, a Dolby Digital AC-3 audio decoder, and a complete digital-video back end for letterbox and pan-and-scan support.

The programmable RISC engine described by Oak's Wen Hsu consists of a simple 32-bit scalar CPU core with 64 32-bit registers, supporting 32K of instruction space and 1K of data. It operates at 67.5 MHz with a three-stage pipeline. Because of the short pipeline, Hsu claims there is no penalty for any type of branch operation, load, or store.

The chip would connect directly to 2M of SDRAM, an audio DAC, an analog video encoder, an 8/16-bit host CPU, and the DVD drive's controller chip. No other significant components would be needed to make a complete DVD player. This system would cost less than a player based on a set of discrete MPEG-2 audio and video decoder chips.

Oak says that such a chip could be fabricated in 0.35-micron CMOS, operating from a 3.3-V supply with 5-V-tolerant I/O, and packaged in a 160-pin PQFP. No specific product plans were disclosed, however.

Media processors from Samsung and Philips can also be used in DVD players, but the higher performance and floating-point support in these parts is likely to make them too expensive for this application. Like Oak, Fujitsu has targeted the DVD market for its MMA chip *(see* **101502.PDF***)*, which was announced at the Forum. MMA's more flexible design may make it easier to adapt to the evolving DVD standard, but Oak's simpler design may be less expensive. Given Oak's unwillingness to discuss an actual product, it appears Fujitsu will reach the market first. —*P.N.G.*

TriTech Debuts Highly Integrated 3D Accelerator

The TR25201 3D graphics controller, part of TriTech's new Pyramid3D product family, is the first 3D chip for the personal-computer market to include integrated hardware support for geometry, setup, and rendering in a single device. This combination lets the device offload from the host processor all parts of the 3D pipeline except scene definition.

The result is high-performance and high-quality rendering. TriTech rates the TR25201 at 1M triangles/s (for 25-pixel shaded, textured, fogged, and Z-buffered triangles). The part also provides hardware support for radiosity-based lighting, trilinear MIP-mapped and bump-mapped textures, Phong shading, and complex shading effects such as environment mapping. A PCI interface and integrated 200-MHz RAMDAC are also included, supporting 1,600 × 1,200 resolution.

Microsoft's Direct3D API does not yet allow application developers to take advantage of all the features of Pyramid3D. TriTech is working directly with several ISVs to develop targeted software and with Microsoft to extend Direct3D. Even within the current constraints of Direct3D, the TR25201 is said to offer faster rendering than the other 3D chips in its price range.

Another unique feature of the TR25201 is support for

multichip configurations. In theory, up to 10 TriTech devices can be interconnected to share the 3D rendering process. TriTech claims each chip requires only about 10% of a Pentium-100 processor for scene management, eliminating a common bottleneck in most other 3D accelerators.

Two independent 32-bit SGRAM buses support local memory. TriTech believes the dual buses provide better overall performance than a single 64-bit bus. Up to 32M of SGRAM can be attached, enabling high-resolution frame and Z buffers as well as local texture storage.

TriTech *(www.tritech-sg.com)* also offers the TR25202, which lacks the geometry processor and is less expensive than the TR25201. Both parts are packaged in 304-ball BGA packages and are expected to be in production in 2Q97. Pricing is estimated at $70 for the TR25201 and $50 for the TR25202, both in 10,000-unit quantities. —*P.N.G.*

S3 Upgrades Popular 3D Accelerator

After shipping three million units of its original Virge 3D chip, representing 70% of the market for PC 3D adapters, S3 has announced two new parts that offer three times the basic rendering performance and significantly improved display quality at about the same price point. Like their predecessor, these chips offer low-end 3D acceleration at essentially no premium over a fast 2D graphics chip. The new chips lag well behind the performance of more expensive 3D accelerators, however, many of which include setup engines.

The Virge/DX and Virge/GX graphics chips are identical except for their frame-buffer DRAM controllers: the DX supports EDO DRAM, while the GX also supports SDRAM and SGRAM. Both provide perspective correction and trilinear MIP-mapped texturing without a performance penalty. Turning on these quality enhancements on the older Virge resulted in a dramatic drop in frame rate.

The new parts achieve their rated 3× performance improvement using a significantly improved rendering pipeline that also provides better support for large triangles, reducing the host-CPU overhead for setup processing. The S3 chips do not, however, completely offload the 3D setup process, preventing them from matching the performance of midrange and high-end 3D accelerators.

Both the DX and the GX support up to only 4M of local memory, limiting the amount of texture storage to 1.25M in a typical 800 × 600 double-buffered configuration with 16-bit color and Z-buffer support. Given the dramatic reductions in memory prices over the past year, 8M configurations are becoming more popular, although perhaps not at the price points S3 focuses on.

The new parts also include S3's 2D and video accelerator engines, and they are compatible with the software drivers and 208-pin PQFP packages of the earlier Virge chip, as well as S3's Trio family of 2D accelerators. Pricing for the Virge/DX and Virge/GX is $28 and $29, respectively, in 10,000-unit quantities. Both chips are now sampling, with volume production scheduled for 4Q96.

We expect the "free-D" approach embodied in S3's Virge, ATI's 3D Rage, and other low-cost graphics chips will become the standard solution for 3D in low-end systems, while integrated setup and geometry engines will provide key differentiating features for lower-volume midrange and high-end 3D products. —*P.N.G.*

VLSI SongBird Leads Audio Migration to PCI

The VL82C829 SongBird 3D audio accelerator from VLSI is the first PCI-based accelerator to support Microsoft's DirectSound 3D API and legacy SoundBlaster audio, and one of the first audio controllers that connects to an external analog codec using Intel's AC '97 interface *(see* **1009MSB.PDF***)*.

SongBird includes a fixed-point DSP to implement a full range of sound effects, including the head-related transfer function (HRTF) algorithm used to create true 3D positional audio using only two speakers. The DSP gives SongBird a significant performance advantage over emerging software-based audio implementations. According to the company, a software-only HRTF implementation requires more than half of a Pentium-166 processor.

The chip is packaged in a 208-pin MQFP or TQFP. It includes interfaces for PCI, optional SRAM for reverb effects, a joystick, an external Dolby AC-3/MPEG audio decoder, and the external codec. Sampling is scheduled to begin in 1Q97 with production in 2Q97. Pricing is $25 each in 10,000-unit quantities. —*P.N.G.*

Motorola 68376 Flies as TouCan

Motorola's new 68376 is the first in a promised series of 68K-based microprocessors to include a CANbus controller. The part is sampling now, with production set for 1Q97. Called TouCan, the line of controllers extends the reach of Motorola's popular 68300 family further into high-end automotive applications. Volvo, for one, has committed to use the part in future models.

The CAN (controller-area network) specification has gained popularity in automotive and industrial applications because of its deterministic response, resistance to EMI, and simple wiring topology. Currently, most vendors implement CAN interfaces with separate chips; the '376 is the first part from Motorola to integrate CAN onto the microprocessor.

The '376 includes the usual set of 68300-family peripherals, including the timing-processor unit (TPU), queued serial module (QSM), configurable timer module (CTM), and 10-bit A/D converter. The part also has a relative abundance of memory: 8K of mask ROM, 4K of general-purpose SRAM, and nearly 4K more SRAM for the TPU. The complex TPU and the large ROM make the '376 attractive for automotive manufacturers. In a 160-lead QFP, the chip lists for $27.16 in 10,000-unit quantities. —*J.T.* M