PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,535,346

Data processor with future file with parallel update and method of operation
Issued: July 9, 1996
Inventor: Thomas L. Thomas, Jr.
Assignee: Motorola
Filed: July 5, 1994
Claims: 20
A data processor with a future file and a method of operating it. The processor has multiple architecturally visible registers, an execution unit, a rename buffer, and a future file. The rename buffer stores a result of the instruction and copies the result to the architecturally visible registers in response to instruction completion. The future file has multiple entries, each storing the most recent value of the architecturally visible registers. The most recent values are determined with respect to the series of instructions. Each of the entries provides the most recent value to the execution unit as an operand. Each of the entries also stores a value of the architecturally visible registers when an exception occurs.

5,530,941

System and method for prefetching data from a main computer memory into a cache memory
Issued: June 25, 1996
Inventors: Pirmin L. Weisser, et al
Assignee: NCR
Filed: August 6, 1990
Claims: 13
On a bus with multiple bus masters, a broad method of prefetching information predicted to be used from a main memory into a cache memory such that none of the system access requests from the bus masters will be delayed.

5,530,890

High-performance, low-cost microprocessor
Issued: June 25, 1996
Inventors: Charles H. Moore, et al
Assignee: Nanotronics (now Patriot Scientific)
Filed: June 7, 1995
Claims: 10
A stack-based microprocessor containing a central processing unit, a separate DMA processing unit, and an on-chip DRAM controller. The highly integrated microprocessor is designed to reduce system costs by reducing external chip counts.

5,530,825

Data processor with branch target-address cache and method of operation
Issued: June 25, 1996
Inventors: Bryan P. Black, et al
Assignee: Motorola
Filed: April 15, 1994
Claims: 4
A processor with a branch target-cache. The branch target-cache is accessed by the fetch address of the current instruction. The fetch address is a four-instruction address. The cache contains a tag identifying one of the four instructions at the fetch address to which the entry corresponds. The target address becomes the predicted address if the tag matches the offset into the fetch address of the current instruction.

5,530,817

Very large instruction word type computer for performing a data transfer between register files through a signal line path
Issued: June 25, 1996
Inventor: Yoshio Masubuchi
Assignee: Toshiba
Filed: February 22, 1993
Claims: 11
A very large instruction word (VLIW) computer architecture in which the instruction word is divided into operation-field groups. Each field is executed by an independent processor. The computer contains independent register files for each of the respective processors. Data transfer between register files is directed by a command included as an operation for at least one of the processors.

5,530,804

Superscalar processor with plural pipelined execution units, each unit selectively having both normal and debug modes
Issued: June 25, 1996
Inventors: Gregory C. Edgington, et al
Assignee: Motorola
Filed: May 16, 1994
Claims: 42
A superscalar pipelined processor in which each of the superscalar execution units is capable of executing in a debug address space in debug mode and a normal address space in normal mode. The debug mode executes instructions to debug the CPU at substantially the same speed as the normal mode.

OTHER ISSUED PATENTS

5,534,796 *Self-clocking pipeline register*
5,530,891 *System-management interrupt mechanism within a symmetrical multiprocessing system*
5,530,824 *Address translation circuit* M