PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,544,082

Method and system for placing a computer in a reduced power state
Issued: August 6, 1996
Inventors: Fernando Garcia-Duarte, et al
Assignee: Microsoft
Filed: February 15, 1995
Claims: 53
A method and system for placing a computer in a reduced power state is provided. In one embodiment of the invention, the system monitors the performance of some monitored activity (e.g., the idle activity) of a program executing. The system determines whether the program is performing the monitored activity regularly. If the program is performing the monitored activity regularly, the system places the computer in a reduced power state.

RE35,311

Data-dependency-collapsing hardware apparatus
Issued: August 6, 1996
Inventors: Stematis Vassiliadis, et al
Assignee: IBM
Filed: August 18, 1994
Claims: 46
A multifunction ALU (arithmetic/logic unit) for use in digital data processing facilitates the execution of multiple arithmetic operations in parallel, thereby enhancing processor performance. The proposed apparatus reduces the instruction-execution latency that results from data-dependency hazards in a pipelined machine. This latency reduction is accomplished by collapsing the interlocks caused by these hazards. The apparatus achieves performance improvement while maintaining compatibility with previous implementations that use an identical instruction-set architecture.

5,542,109

Address tracking and branch resolution in a processor with multiple execution pipelines and instruction-stream discontinuities
Issued: July 30, 1996
Inventors: James S. Blomgren, et al
Assignee: Exponential Technology
Filed: August 31, 1994
Claims: 10
An address of any desired instruction in a superscalar processor is generated using address-tracking logic. A sequential address register in the last stage of the processor's pipelines holds the address of the oldest instruction in the pipelines. This register is updated with a target address when a branch instruction is actually taken. A branch resolver uses the address-tracking logic to generate the address of a branch instruction being resolved and the address of the following sequential instruction. A recovery address for branch misprediction sent to the instruction fetcher is the following sequential address when the branch is actually not taken and the target address when the branch is actually taken. The branch can be resolved in any pipeline stage.

5,542,059

Dual instruction-set processor having a pipeline with a pipestage functional unit that is relocatable in time and sequence order
Issued: July 30, 1996
Inventor: James S. Blomgren
Assignee: Exponential Technology
Filed: December 21, 1994
Claims: 16
A CPU pipeline is able to process instructions from a complex instruction-set computer CISC instruction set and from a reduced instruction-set computer RISC set, as determined by a mode register. Two instruction-decode units are used, one for each instruction set. Compound CISC instructions use a typical five-stage pipeline. When the CPU switches to RISC mode, the pipeline is rearranged for processing the simpler RISC instructions, reducing the latency for simpler RISC instructions.

5,542,058

Pipelined computer with operand context queue to simplify context-dependent execution flow
Issued: July 30, 1996
Inventors: John E. Brown III, et al
Assignee: DEC
Filed: October 4, 1994
Claims: 20
A pipelined microprocessor chip adheres to strict read-and-write ordering by sequentially buffering operands in queues during instruction decode, then removing the operands in order during instruction execution. Any instruction that requires additional access to memory inserts the requests into the queued sequence (in a specifier queue) such that read-and-write-ordering is preserved. The synchronization method allows overlap of execution.

OTHER ISSUED PATENTS

5,542,075 *Method and apparatus for improving performance of out-of-sequence load operations in a computer system*
5,542,033 *Correction and modification of microprocessor chip operations* M