MOST SIGNIFICANT BITS

MoSys and Rambus Bury Hatchet

In an unexpected but welcome move, MoSys and Rambus have announced plans to codevelop a new high-performance RDRAM chip for graphics products and other high-end applications. The new MoSys RDRAMs combine the best technology from each company: the high-bandwidth interface from Rambus *(see* **070304.PDF***)* and the low-latency, multibank MDRAM core from MoSys *(see* **091703.PDF***)*.

The two companies have been rivals in the graphics-memory market. The Rambus architecture was unveiled in 1992 but began to achieve commercial success only in 1996. The revolutionary RDRAM bus interface offers high peak bandwidth and excellent expandability, but RDRAMs remain hampered by a fairly conventional DRAM core.

The MoSys MDRAM solved the latency problem with a revolutionary core design based on many small (32K) blocks. The MDRAM core, however, is handicapped by an inflexible bus interface with limited scalability, and MoSys has done much less work than Rambus to develop efficient and manufacturable PC-board layouts.

Rambus has been the clear winner in the market so far. The company is especially proud of its design win in the popular Nintendo 64 video game. RDRAMs are also used with Cirrus Logic's Laguna graphics chips, the Chromatic Mpact media processor, and other products. Over $400 million in Rambus-compatible ICs have been sold to date. By comparison, the only design win for MDRAMs in the PC market is for a Tseng Labs graphics controller.

The companies did not announce a name for the MoSys RDRAM; we would enjoy MRDRAM. Other details of the new part are also unavailable. Rambus said it plans to increase the RDRAM transfer rate beyond the current 600 Mbytes/s to provide a better match to the MoSys core's internal 1-Gbyte/s bandwidth. Apart from this change, the new parts will remain compatible with current RDRAMs, offering an upgrade path to existing RDRAM customers.

Rambus will continue to develop faster versions based on its own core; these parts will be sold by current Rambus licensees Hitachi, Hyundai, LG, NEC, Oki, Samsung, and Toshiba. Under the agreement, the MoSys RDRAM will be sold only by MoSys; other Rambus licensees do not gain access to the MDRAM core.

Neither MoSys nor Rambus is discussing possible applications for MoSys RDRAM technology as part of the recently announced Intel/Rambus nDRAM initiative *(see* **1017MSB.PDF***)*. We believe technology would be a natural fit for the initiative, now rechristened Direct RDRAM. The multibank MoSys core is a good match for the multithreaded nature of modern operating systems, especially those under development for Merced, the presumed beneficiary of Direct RDRAM's increased performance. —*P.N.G.*

Samsung Proposes Next-Generation SDRAM

Establishing an alternative to the future Intel/Rambus Direct RDRAM, Samsung has announced SDRAM-II. The proposal doubles the data-transfer rate of current SDRAMs by presenting data on each edge of the memory clock. The new chips also generate an "echo clock" during reads to ensure proper synchronization between clock and data. Both techniques have been used by Rambus since 1992.

Samsung plans to offer SDRAM-II devices in 64-Mbit through 1-Gbit densities, with bus widths of 4 to 32 bits. Clock speeds of up to 150 MHz will yield transfer rates up to 1.2 Gbytes/s per device, or 2.4 Gbytes/s for a typical 64-bit-wide memory array. The electrical interface is based on the stub series-terminated logic (SSTL) standard.

Samples of the 64-Mbit SDRAM-II are scheduled for 4Q97, with production starting in mid-1998. Samsung plans to offer fully tested board-level reference designs. The DRAM maker is also working with unspecified chip-set vendors to provide support for SDRAM-II, but Intel—the highest-volume chip-set vendor in the world—has no plans to support SDRAM-II with its own chip sets, preferring to remain focused on the Direct RDRAM effort.

Extending SDRAM chip sets for SDRAM-II will be relatively simple. In contrast, chip sets for Direct RDRAM—like current Rambus chip sets—will require a Rambus license and may not be available from all ASIC vendors. On the other hand, an SDRAM-II interface will require about 80 more pins than a Direct RDRAM interface, roughly offsetting the cost of the RDRAM controller license.

We expect to see some chip-set makers use SDRAM-II to stretch the life of their designs by another year or two, but in the long run, Direct RDRAM is likely to take over the market for PC main memory. —*P.N.G.*

Intel 430TX Spans Notebook, Desktop

Showing what may be the company's last major chip set for Pentium systems, Intel has unveiled the 430TX, bringing full support for the advanced configuration and power interface (ACPI) specification to notebook and desktop Pentium systems. The 430TX builds on the earlier 430HX and 430VX desktop chip sets *(see* **1016MSB.PDF***)* with im-proved power management, 33-Mbyte/s UltraDMA to the hard disk, and an SMBUS controller. BGA packaging reduces the footprint from previous designs.

Through Intel's dynamic power-management architecture (DPMA), the new chip set consumes significantly less power than the earlier 430MX mobile chip set: just 400 mW typical compared with as much as 1.6 W for the 430MX *(see* **091301.PDF***)*.

The 430TX works with an upgraded version of Intel's 380 Dock Set *(see* **1005MSB.PDF***)* to provide hot docking and complete power management for notebook systems. The new

82380FB PCI-to-PCI bridge increases peak transfer rates to 100 Mbytes/s.

The 430TX is less of an advance for desktop systems, but corporate users will appreciate the power savings and remote-management capabilities of ACPI, and even home-entertainment PCs may take advantage of ACPI for instant-on operation and other features.

The 430TX chip set consists of the 82439TX (providing cache, DRAM, and PCI interfaces) and the 82371AB (ISA, USB, IDE, and SMBUS interfaces). Both are packaged in a 324-pin BGA package; the chip set is in production now and is priced at $32.50 in 1,000-unit quantities. The revised 380 Dock Set is also in production at $28. —*P.N.G.*

Intel's i960RD Hits 66 MHz

After more than a year, Intel has added a new member to its i960 family. The new i960RD-66 is similar to the i960RP *(see* **090802.PDF***)* but uses a clock-doubled core that hits 66 MHz. Like its predecessor, the 'RD is intended to handle disk and network I/O for high-end servers.

The i960R-series, which began with the 'RP in 1995, signals a fundamental shift in Intel's strategy for the i960 line. The company is now emphasizing application-specific I/O rather than simple CPU power consumption, performance, or price—three characteristics by which the previous chips were never distinguished. By targeting server I/O bottlenecks, Intel differentiates its i960 chips and, not coincidentally, raises the performance of Pentium Pro–based servers.

The i960RD (code-named Kaibab) is pin-compatible with the 'RP, although the new chip runs at 3.3 V with 5-V-tolerant I/O. The new supply voltage, which halves power consumption, was enabled by moving to Intel's 0.5-micron process. More minor improvements include reduced PCI-bridge latency, better interrupt handling, and support for additional private devices on the PCI bus.

Intel is sampling the chip now; production is set for 2Q97. The company charges twice the price for twice the speed: $100 for the i960RD-66 versus $50 for the 'RP-33. Intel anticipates only minor changes to the i960 line this year before a more substantial change sometime in 1998. —*J.T.*

Silicon Magic Merges DRAM and 2D Graphics

Following the path of NeoMagic *(see* **090304.PDF***)*, Silicon Magic (*www.simagic.com)* and partner Oki have announced the F/X256, a single-chip 2D graphics controller with an integrated 1.25-Mbyte frame buffer.

The new part provides a high level of integration, combining a VGA core, a 2D GUI accelerator, MPEG-1 video and audio decoders, a video-capture port, a 135-MHz RAMDAC, and digital audio output with the 40K×256-bit memory array running at 80 MHz. Some customers will choose to supplement the fast (2.6-Gbyte/s) on-chip memory array with 1M of slower off-chip SDRAM memory, sacrificing much of the chip's 2D speed in exchange for true-color graphics at 1024 × 768 resolution.

The key advantages of an embedded frame buffer—reduced footprint and power consumption—apply mainly to the laptop market, where NeoMagic has been successful. The F/X256 offers a small footprint—a single 208-pin PQFP package plus one optional SDRAM—but does not include LCD support. This shortcoming limits its use to desktop systems, where integration and power consumption are much less important than performance, expandability, and advanced features like 3D acceleration. Silicon Magic describes its target market as the "professional desktop," but MPEG hardware decoding is not particularly valuable there, especially since current Pentiums can decode MPEG-1 in software.

The most likely market for the F/X256 is integrated graphics on motherboards for servers and low-end desktops. Priced at $35 in volume, the chip is unlikely to undercut the price of discrete implementations based on low-end 2D controllers that sell for less than $20. In effect, Silicon Magic is charging about $12 per megabyte for its integrated memory, well above the going rate for separate DRAMs.

The F/X256 is an interesting part and may find some customers, but it may ultimately be most valuable as a test vehicle for Oki's embedded DRAM technology. We expect Silicon Magic, by combining a fast on-chip frame buffer with a good 3D accelerator, to create much more interesting products in the future. —*P.N.G.*

RISC Growth Slowed in 1996

According to new sales figures from analyst Andrew Allison *(www.aallison.com)*, revenue from RISC systems grew by 24% in 1996, compared with a growth rate of 42% in 1995. This growth was driven by increased demand for RISC servers; Allison estimates revenue from RISC workstations was flat last year, with unit sales declining by 5–10%. RISC workstations are under pressure from high-end x86/NT-based systems, and this combination is likely to cause RISC workstation sales to decline further in 1997.

	1996		1995		Annual Growth
	Share	Revenue	Share	Revenue	
1) PA-RISC	30%	$15.3 B	30%	$12.5 B	+22%
2) PowerPC*	27%	$14.2 B	28%	$11.8 B	+20%
3) SPARC	17%	$8.8 B	17%	$6.9 B	+28%
4) MIPS	16%	$8.2 B	16%	$6.8 B	+21%
5) Alpha	9%	$4.6 B	6%	$2.5 B	+84%
6) Other**	1%	$0.6 B	3%	$1.2 B	–50%
	100%	**$51.7 B**	**100%**	**$41.7 B**	**+24%**

*includes POWER **includes Clipper, 88K, and others

Revenue from Digital's Alpha systems increased by 84% last year, to $4.6 billion. This growth still leaves Alpha at about half the size of SPARC and MIPS and well behind PowerPC and PA-RISC, the leader at $15.3 billion. Despite a significant increase in unit volume, PowerPC lost ground to PA-RISC. The bulk of the new PowerPC units were relatively low priced Macintosh systems; slow sales at IBM prevented PowerPC from gaining share in dollar terms. —*L.G.*