PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,557,763

System for handling load and/or store operations in a superscalar microprocessor
Issued: September 17, 1996
Inventor: Cheryl D. Senter, et al
Assignee: Seiko Epson
Filed: June 5, 1995
Claims: 24
A system and method for managing load and store operations necessary for reading from and writing to memory or I/O in a superscalar RISC processor. It provides a load/store unit whose main purpose is to complete load requests out of order whenever possible to get the load data back for use by an instruction-execution unit as quickly as possible. A load operation can be performed out of order only if there are no address collisions and no writes pending. An address collision occurs when a read is requested at a memory location where an older instruction will be writing.

5,555,429

Multiport RAM-based multiprocessor
Issued: September 10, 1996
Inventor: Ward D. Parkinson, et al
Assignee: Micron Technology
Filed: May 8, 1995
Claims: 11
An integrated circuit chip includes a random access memory (RAM) array, serial access memory (SAM), an arithmetic logic unit, a bidirectional shift register, and masking circuitry. The arithmetic logic unit, SAM, shift register, and masking circuitry are all as wide as one side of the RAM array and can all communicate with each other via data-transfer means. This allows wide data processing, user-configurable for parallel processing. Bits masked by the masking circuitry are selectable by data in the bidirectional shift register, providing shiftable masking means. Random access and serial access are done through separate ports.

5,555,424

Extended Harvard-architecture, computer-memory system with programmable variable address increment
Issued: September 10, 1996
Inventor: Edward R. Sederlund, et al
Assignee: Dow Chemical
Filed: October 6, 1994
Claims: 9
An extended Harvard-architecture memory system with an address memory for containing an ordered sequence of program-memory addresses and a value memory for containing a series of related data-value sets. Each of the addresses contained in the address memory is associated with a distinct set of instructions, such as a subroutine, that is contained in the program memory. The address memory may also contain the address of one or more instruction parameters contained in the value memory or in a separate data memory. The value memory also includes a logic interface to enable multiple different address increments to be programmably selected.

5,555,423

Multimode microprocessor having a pin for resetting its register without purging its cache
Issued: September 10, 1996
Inventor: Edward T. Grochowski, et al
Assignee: Intel
Filed: July 26, 1995
Claims: 12
In an x86 microprocessor, a switch from protected mode to real mode requires a pseudo-reset of the processor. This invention provides a specific implementation of the INIT pin that causes most of the processor to be reset as if RESET were asserted but leaves the internal cache and floating-point registers unchanged.

5,555,384

Rescheduling conflicting issued instructions by delaying one conflicting instruction into the same pipeline stage as a third nonconflicting instruction
Issued: September 10, 1996
Inventor: David B. Roberts, et al
Assignee: Silicon Graphics
Filed: October 18, 1994
Claims: 19
Methods and apparatus for optimizing an instruction pipeline in a computer using a pipeline controller that has functions at the beginning and end of the pipe. The controller monitors data availability of floating-point data at the beginning of the pipe. Based on the availability of data, certain instructions are allowed to proceed or not. At the end of the pipe, the controller monitors all instructions in the pipeline, notes all potential resource conflicts, and resolves these potential conflicts by either the insertion of an appropriate number of hold states or the conclusion that no actual resource competition exists.

OTHER ISSUED PATENTS

5,557,760 *Integrated circuit data processor including a control pin for deactivating…*
5,555,400 *Method and apparatus for internal cache copy* M