Digital to Ship 600-MHz Alpha

Raising its defenses against potential challengers to its performance throne, Digital Semiconductor has announced it is sampling a 600-MHz version of its 21164 Alpha processor, with volume production slated for July. The new part clocks 20% faster than the current 500-MHz chip, which delivers better integer performance than any other microprocessor available today. Digital claims the 600-MHz 21164 will deliver 17 SPECint95 (base) and 25 SPECfp95 (base) while dissipating 30 W (maximum).

HP still hopes its forthcoming PA-8200, due at about the same time as the 600-MHz Alpha chip, will grab the performance lead. HP expects its new chip to reach 15.5 SPECint95 (base) and 25 SPECfp95 (base). This race is too close to call until actual measured results are posted by both vendors. Digital's 600-MHz chip should easily fend off speed upgrades of the R10000, UltraSparc, and other processors expected later this year.

The 20% speed boost comes from process and yield improvements; the basic design of the 21164 has not been changed. The increase bodes well for the 21264, which Digital hopes will achieve similar clock speeds, although the company has conservatively committed to only 500 MHz for its next-generation part. Digital did not reveal pricing for the 600-MHz device; we expect it to be about $3,000, the vendor's usual price for its fastest parts. —*L.G.*

NEC's R4102 Boosts Speed to 66 MHz

NEC has released the R4102, the follow-on to its R4100 and R4101 MIPS processors (see MPR 7/8/96, p. 5). The new device, which is sampling now, is similar to its predecessors but boosts the top clock speed from 40 MHz to 66 MHz. The new device will be priced at about $25 in quantity when it begins production in 3Q97.

Differences between the R4101 and R4102 are minor. The newer device has a larger, 4K instruction cache in addition to its 1K data cache. The R4102 also has a wider, 32-bit external data bus. The wider bus and larger cache should help keep the 4102's core from starving at the higher clock rate. The chip also adds A/D and D/A converters. At about 250 mW, power consumption is comparable to the R4101's.

In all, these enhancements should make the R4102 a welcome performance upgrade for vendors (such as NEC itself) making handheld PCs running Windows CE. The analog circuitry replaces external logic for the touchscreen and simple audio these units require, and the faster core frequency, larger cache, and wider bus will improve performance noticeably. NEC is particularly keen to replace PCMCIA modem cards—which the current MobilePro and related units now use—with a software-only modem. The company claims a 28.8-kbps V.34 modem can be implemented entirely in software on the new processor.

NEC has been aggressive in pushing its MIPS chips into the embedded market, devoting its best 0.35-micron fab processes to the R4100 and R4300 series of chips. This strategy is paying off, giving NEC an edge in economics (through smaller die sizes) and specifications (through lower power consumption and higher clock rates). The company is well positioned to continue pushing its advantages into more high-volume applications. —*J.T.*

LSI Logic, Philips Join ARM Band

As the river turns to a flood, two more semiconductor vendors have acquired licenses to ARM's embedded microprocessor technology, *Microprocessor Report* has learned. The latest converts are Philips Semiconductor and LSI Logic; both, coincidentally, are also MIPS licensees. Like Motorola (see MPR 3/31/97, p. 4), neither vendor plans to publicly announce its ARM deal for some time. LSI's arrangement is presumably at the behest of a customer wanting to combine an ARM core with LSI's renowned ASIC technology.

In Philips's case, the company's telecommunications products group in Zürich will develop application-specific chips around the ARM core to be sold under the Philips name. The chips will be tailored for wireless communications, a market segment where ARM and Philips have both been strong. In keeping with recent company trends, roughly 15% of the devices should appear in Philips's own products; the rest will be sold on the open market. With TriMedia, MIPS, and now ARM, Philips seems well equipped to deal with whatever new consumer items come its way.

With most major microprocessor vendors and ASIC suppliers in the world already on board, ARM's prospecting list must be getting short. Unless its starts another chip company to sell its wares to, ARM will have to broaden its focus. We expect the company will approach vendors of design tools such as Cadence, Mentor, and Synopsys. Not coincidentally, all three companies (and ARM) are members of the Virtual Socket Interface (VSI) Alliance, an industry group dedicated to promulgating the use of intellectual property in designing application-specific circuits.

To appeal to CAE vendors, ARM may have to provide a synthesizable "soft" version of its eponymous processor core. Currently, all ARM cores are delivered as hard macros tailored for individual manufacturing processes. Indeed, ARM charges its licensees separately for each individual process generation of its cores. A synthesizable version would promote more widespread use of the ARM architecture but would also trade off some performance and die area for flexibility.

With ARM becoming so profligate with its licensing, it isn't clear how the current partners can differentiate themselves. A portable, synthesizable, and widely available version could only make the competition more fierce. —*J.T.*

Rockwell Signs On as New PicoJava Licensee

At the recent JavaOne conference, Sun Microelectronics announced one new licensee and a partnership agreement. Both deals are intended to extend PicoJava's reach into specialized niches where Sun has no application experience.

Rockwell Collins brings the list of publicly proclaimed PicoJava partners to five. The company brings with it its low-power design methods and experience in wireless communications, global-positioning systems, and avionics. No specific chip plans were announced, but Rockwell expects to pursue development of Java-enabled personal communicators and, ominously, aircraft guidance systems.

A separate deal with Toshiba's notebook PC operation calls for development of one or more low-power devices for portable Java systems. Toshiba is not a licensee; instead, the Japanese company will provide design input to Sun, which will retain exclusive rights to sell the resulting chips worldwide. The device will be built by an unnamed foundry and sold under the Sun Microelectronics brand name.

Of the first four PicoJava licensees, NEC and LG Semicon have signed their agreements; Mitsubishi and Samsung are covered by only letters of intent (see MPR 6/17/96, p. 4). Counting Sun itself, Rockwell brings the number of active developers to four. Partner LG plans to ship its first chips later this year in Internet-enabled TVs and other LG-branded consumer goods. LG will build chips in its own fabs, but, as with the Toshiba deal, Sun retains chip-marketing rights.

Work on Sun's own MicroJava chip continues. The company expects first silicon shortly before the end of this year, with production in mid-1998. MicroJava is expected to be little more than a PicoJava core with a memory interface (see MPR 10/28/96, p. 28). In twelve months, there should be enough Java processors available to give eager hardware engineers their first real taste of native Java performance. —*J.T.*

MoSys Debuts High-Speed SGRAM Cache

MoSys, which recently announced a licensing arrangement with Rambus that allows MoSys to produce faster (but still pin-compatible) RDRAMs, has now entered another part of the graphics-memory market with a new high-performance device compatible with SGRAM. The new MG802C256 is a 256K × 32-bit SGRAM that operates at up to 150 MHz, making it 50% faster than existing SGRAMs. At that speed, each part achieves 600 Mbytes/s of peak bandwidth. With row and column access times 40% below competing SGRAMs, the new part also provides lower latency than any alternative.

The MG802C256 uses the same multibank core found in MoSys MDRAMs, and the company says that a 128-bit configuration will provide a sustained transfer rate in excess of 2 Gbytes/s. In addition, the new part provides a brief 5-ns T_{CO} (clock to data out) delay, simplifying the board designer's task compared with handling current SGRAMs with 9-ns T_{CO} times out of a 10-ns clock cycle.

The MG802C256 is sampling now, with volume production in May. Speed options are 100, 125, and 150 MHz, with pricing starting at $10.50 in 1,000-unit quantities. The parts are available in 100-pin PQFP and LQFP packages.

MoSys has also begun volume shipments of its new single-chip 256K L2 cache chip, the MC80232k64. The part is organized as 32K × 64 bits and replaces two of the commonly used 32K × 32-bit SRAMs used in Pentium systems today. Like the MG802C256, the MC80232k64 uses the MoSys MDRAM core, significantly reducing board space and power consumption compared with current SRAM-based L2 cache chips.

MoSys says the MC80232k64 consumes only 10% of the power of a 256K SRAM cache, while the single-chip 128-pin LQFP package requires only half the board space of the SRAM alternative. The MC80232k64 also operates at temperatures up to 80°C, somewhat simplifying thermal management in high-performance notebook computers.

The new part is supported by Intel's 430VX, HX, and TX chip sets, as well as offerings from other core-logic vendors. The pinout is a superset of the JEDEC 64-bit PBSRAM standard, making it possible for OEMs to design a single motherboard that supports PBSRAMs or the MC80232k64. The new chip, available in 66-MHz and 75-MHz speed grades, is priced from $6.50 in 1,000-piece lots. —*P.N.G.*

S3 Introduces Third-Generation 3D Chip

S3's new Virge/GX2 shares some of the features of ATI's 3D Rage Pro (see MPR 3/31/97, p. 15), such as a 100-MHz SGRAM frame-buffer interface and a DVD-quality video-scaling engine, but lacks key elements of the ATI design. For example, the Virge/GX2 does not include a setup engine or DVD motion compensation, and its AGP interface supports only the 1× mode without pipelining.

S3 offers instead its unique and potentially valuable DuoView feature, which permits a single frame buffer and graphics controller to drive two displays. This ability is provided by a second output port capable of driving TVs or LCDs with timing requirements different from (or the same as) those of the primary RGB monitor. DuoView will be especially useful in living-room PCs and for presentation graphics on notebook computers.

While ATI's 3D Rage Pro provides an internal 230-MHz RAMDAC and supports even faster RAMDACs when used with a WRAM frame buffer, S3's part works only with its internal 170-MHz RAMDAC. This shortfall, combined with the lack of an on-chip setup engine, will limit the Virge/GX2 to mainstream PC designs and leave the higher-performance, higher-margin applications to the ATI part. On the other hand, the Virge/GX2 is somewhat less expensive, at just $29 in 10,000-unit quantities; this lower price will help compensate for its smaller feature set.

S3 says the Virge/GX2 is sampling now and expects volume production in 2Q97. Diamond, Number Nine, and STB have all announced plans to use the Virge/GX2 on expansion-card products, and S3 will also pursue motherboard design wins for the new chip. —*P.N.G.* M