Temic SPARClet Takes Aim at Telecom

European Vendor Loads TSC701 With Four-Channel HDLC Hardware

by Jim Turley

Stepping out of the shadows, Temic is pushing a series of SPARC-based chips aimed at networking applications. The first of the French company's SPARClet family is the TSC701, designed for T1/E1 access boards for routers, switches, and base stations. The 701 will be followed in the next 12 months by three new chips, each customized for ISDN, ATM, ADSL, or other telecommunications applications.

Temic is a new company that has been around for a while. The company was formed two years ago by the merger of Matra MHS (France), Telefunken (Germany), Dialog (U.K.), and Siliconix (U.S.) and is ultimately controlled by Daimler-Benz. Matra's SPARC license dates back to 1992, but the 701 marks the first use of it. Temic also does a brisk business in 8051, '251, and other small microcontrollers.

SPARC Core Has Embedded Enhancements

The processor core of the 701 is based on the SPARC V8E specification, a licensed enhancement of the usual V8 design. V8E enhancements include a extra register set that is separate from the usual circle of SPARC register windows. The extra set aids real-time performance and speeds exception handling. Faults, traps, and interrupts automatically switch to the extra register set. Because exception handlers typically do not share arguments with user code, this technique avoids disturbing the normal register windows and potentially saves several stack references.

The 701's internal bus supports split transactions, so reads and writes can be posted to/from the chip's bus-interface logic. Nonblocking loads allow the 701 to continue fetching and executing instructions as long as the code is not dependent on the loaded data. Signed and unsigned multiply-accumulate instructions permit pseudo-DSP massaging of data. Two new instructions, SCAN and SHUFFLE, allow the chip to manipulate bit fields in a single cycle—a useful feature in networking applications. So far, Temic is the only vendor using the V8E version of the architecture.

Multiplication Not Its Strong Suit

The SPARC instruction set includes full 32 × 32-bit multiply instructions, but the 701 implements only a partial hardware multiplier. The chip can perform 32 × 8-bit multiplication in a single cycle; 32 × 32-bit operations require four passes through the multiplier. The repetition is invisible to the programmer, except for the four-cycle latency.

Temic believes the SPARClet's simplified multiplier will not be an issue for most applications. The company's code traces show that most multiply-intensive loops are constrained by data bandwidth, not arithmetic performance. The partial multiplier allows Temic to shave transistors without sacrificing net performance.

The 701's 16K instruction cache and 8K data cache are both lockable. Any or all of the sets of these four-way set-associative caches can be frozen, leaving the remaining portion as an *n*-way cache. Most real-time programmers value lockable caches because they help predictability, but unfortunately few microprocessor vendors provide them.

Peripherals Tell the Story

Although the SPARC core is a good performer at 50 MHz, there's nothing to inherently recommend it for communications-oriented applications. To address the needs of these applications, Temic extended the 701's basic CPU with a number of useful peripherals.

The chip includes timers, a DRAM controller, and four high-speed serial links. Each serial channel supports 8-Mbps transmission with synchronous or asynchronous, point-to-point or multipoint protocols. Temic has also grafted some extra hardware onto the chip for calculating CRC and headers, which alleviate the need to do V.110 HDLC coding and decoding using SPARC instructions.

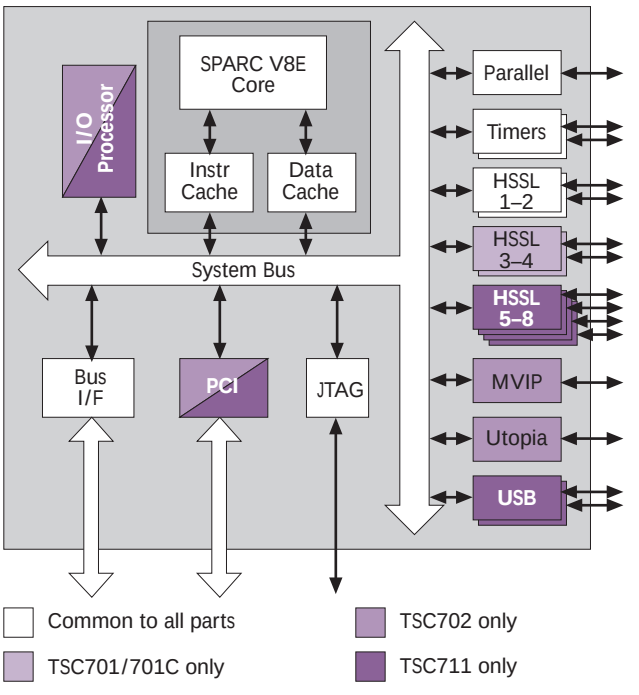

Figure 1. Block diagram shows the differences among Temic's four SPARC-based telecommunications chips. (HSSL=high-speed serial link; MVIP=multivendor integration protocol.)

Price & Availability

The 701 is shipping now at 50 MHz. In 10,000-unit quantities, the chip is priced at $70. For more information contact Temic (Nantes, France) at 33.1.39.44.29.29 or in the U.S. (Santa Clara, Calif.) at 408.982.5885, or visit the Web at *www.temic.de.*

In total, these capabilities allow the 701 to handle four PCM links (T1/E1/E2 or PCM highway) simultaneously or, under ideal conditions, as many as 336 DS0 HDLC channels.

The SPARClet part is fully static—unusual for a SPARC processor—and is built on Temic's 0.6-micron three-layer-metal fab line in Nantes (France). The chip, shown in Figure 2, measures about 10 mm on a side. At 50 MHz, it draws about 1.2 W, fully loaded, from its 5-V supply. Although its power consumption is modest, the 701's static design allows designers to stop the chip entirely when it's not busy, which may eliminate the need for a fan in tightly packed network boxes. The 701 is available in 208-lead PQFP, 209-pin ceramic PGA, or 225-contact BGA packages.

More SPARClet Chips on the Way

Temic's plans call for three more chips in the SPARClet family within a year. They're all similar, as Figure 1 shows, but each has a different mix of peripherals and different cache capacity. The next member will be the 701C, which is due to begin sampling next month. The 701C is much like the 701 but with more protocol-handling hardware and a doubled, 16K data cache in addition to its 16K instruction cache. The 701C will also bump its clock speed up to 66 MHz and its voltage down to 3.3 V, both side effects of a 0.5-micron process shrink.

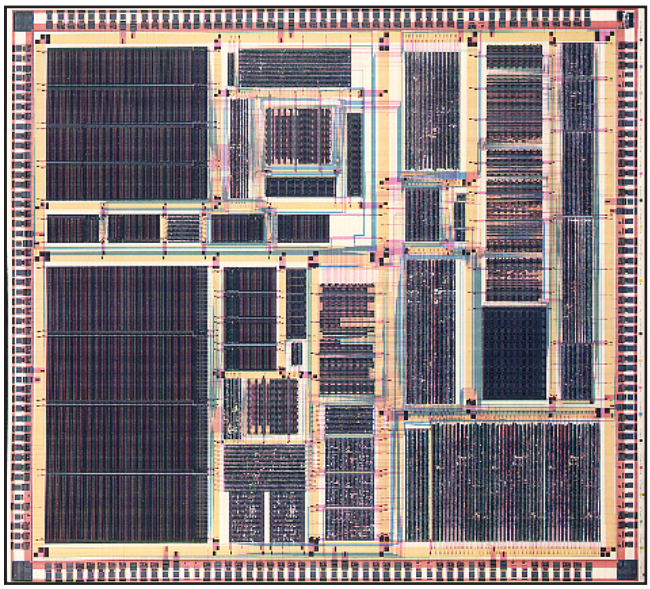

Figure 2. Temic's TSC701 SPARClet processor measures about 100 mm^2 in the company's 0.6-micron CMOS process.

The 711 is a subscriber-side controller for routers, ISDN adapters, and ADSL/HDSL interface boxes. This 66-MHz chip will have a 32K instruction cache and is expected to begin sampling in 3Q97. The part will initially be built by an unnamed Asian foundry in a 0.35-micron process. Temic's own 0.35-micron fab is not due to come on line until 1998.

At the top of the line will be the 702, due to begin sampling in 2Q98. The 702 is tailored for DS3 data rates, supporting eight PCM links and ATM with a Utopia interface. Large, 32K/64K instruction/data caches will allow the chip to run efficiently at 80 MHz. Looking even further out, Temic foresees a 100-MHz, superscalar chip it calls the 801, which is expected to double the performance of the 702.

SPARClet Goes Head to Head With Motorola

Temic is certainly not the first vendor to cast a covetous eye toward networking equipment makers. Network vendors such as Cisco, Bay, and Cabletron have been fickle in the past, using SPARC, MIPS, 68K, and PowerPC chips, among others. In most cases, these have been general-purpose microprocessors used either as "housekeeping" processors, safely out of the data path, or as intelligent data shovels with wide buses and fast clock rates.

Few microprocessors have been specifically equipped to handle data-packet processing. Motorola's 68360 QUICC chip and its big brother, the PowerPC-based MPC860, are two exceptions that have both been successful in this area. The '360 and '860 pack a considerable amount of power in their communications peripherals; the core microprocessor, although not insignificant, is not the major determinant of performance.

At $70 in volume, the 701 sells for at least 20% more than most versions of Motorola's 860 and more than double the price of the 68360. In Temic's favor, the 701 runs at 50 MHz, whereas the best 860 chip runs at 40 MHz; the 68K-based QUICCs are considerably slower. Temic also claims its part can handle four times as many DS0 channels (128) as Motorola's '860. Yet even the '360 can handle Ethernet packets in addition to HDLC and SDLC transmissions, something the faster 701 can't do.

Networking Tide Provides Growth

Instead of becoming yet another general-purpose microprocessor supplier, Temic focused on the needs of one market segment: networking products. The 701 and its stablemates in the SPARClet family devote more silicon to application-specific I/O than to the microprocessor core.

A rising tide raises all boats, and the rise of the Internet has certainly helped float a number of networking companies. While generic microprocessors might score a design win here or another there, they have no guarantee of continued success in this growing and volatile market. With its clear focus and value-added designs, Temic stands a good chance to ride this wave for a while. M