by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,590,357

Integrated CPU core and parallel, independently operating DSP module and time-critical core priority scheme
Issued: December 31, 1996
Inventors: Amos Intrater, et al
Assignee: National Semiconductor
Filed: September 6, 1994
Claims: 2
A processor with a general-purpose CPU and a DSP module has a bus-interface unit for transferring instructions and data on a single external bus. Internally, both the CPU and the DSP module connect to an internal bus that is also shared between instructions and data. The DSP module includes a signal processor for processing a digital signal by executing DSP command-list instructions. The DSP execution is independent of and in parallel with execution of instructions by the general-purpose CPU.

5,588,118

Single-chip dual processor
Issued: December 24, 1996
Inventors: Babu S. Mandava, et al
Assignee: Zilog
Filed: December 23, 1994
Claims: 7
A single-chip dual processor is implemented combining a microcontroller and DSP. A single instruction set is utilized for programming both processors in one source program stored in a single external program memory. The compiler distinguishes which instructions are to be executed by which processor and designates each instruction to be stored in memory in a space allocated to the appropriate processor.

5,584,038

Entry allocation in a circular buffer using wrap bits indicating whether a queue of the circular buffer has been traversed
Issued: December 10, 1996
Inventors: David B. Papworth, et al
Assignee: Intel
Filed: April 7, 1996
Claims: 8
The P6 register-alias table (RAT) unit allocator is described. The allocator assigns entries for the ROB, receives requests to store micro-ops in the ROB, and generates a head pointer to identify a starting entry. The head pointer includes a wrap bit. A tail pointer is generated, including the wrap bit, to identify an ending entry in the ROB. The allocator sequentially assigns entries for the requests located between the head pointer and the tail pointer. The allocator utilizes an all-or-nothing allocation policy such that either all or no incoming instructions are allocated during an allocation period.

5,584,009

System and method of retiring store data from a write buffer
Issued: December 10, 1996
Inventors: Raul A. Garibay, Jr., et al
Assignee: Cyrix
Filed: October 18, 1993
Claims: 16
A superscalar superpipelined microprocessor having a write buffer located between the core and cache is disclosed. The write buffer is controlled to store the results of write operations to memory until the cache becomes available, e.g., when no high-priority reads are to be performed. The write buffer has multiple entries that are split into two circular buffer sections for facilitating the interaction with the two pipelines of the core; cross-dependency tables are provided for each write-buffer entry to ensure that the data is written from the write buffer to memory in program order.

5,584,001

Branch target buffer for dynamically predicting branch instruction outcomes using a predicted branch history
Issued: December 10, 1996
Filed: July 31, 1995
Inventors: Bradley D. Hoyt, et al
Assignee: Intel
Claims: 42
The P6 branch-prediction mechanism is partially described. The mechanism maintains both speculative history and actual history for each branch instruction in a branch-target buffer. The actual branch history contains the branch history for fully resolved occurrences of the branch instruction. The speculative branch history contains the actual history plus the history of recent branch predictions for the branch.

OTHER ISSUED PATENTS

5,590,379 *Method and apparatus for cache memory access with separate fetch-and-store queues*
5,590,352 *Dependency checking and forwarding of variable-width operands*
5,590,296 *Data processor processing a jump instruction*
5,590,295 *System and method for register renaming*
5,588,127 *High-speed microprocessor branch decision circuit*
5,586,284 *Triple-register RISC digital-signal processor*
5,584,037 *Entry allocation in a circular buffer*
5,583,806 *Optimized binary adder for concurrently generating effective and intermediate addresses* M