AUDIO/VIDEO

3D accelerator chip adds a third dimension to 2D graphics. The TEX-1516 chip, jointly developed by Reality Simulation Systems and S-MOS Systems, makes possible workstation-like graphics while delivering peak performance of 150 Mpixels/s. Dave Bursky, *Electronic Design*, 5/1/97, p. 83, 3 pp.

3D graphics chips boost the speed of display controllers. Advances in 3D graphics accelerators give PCs the power to compete with graphics workstations and give customers the ability to use 3D software. Jules H. Gilder and Dave Bursky, *Electronic Design*, 5/12/97, p. 117, 7 pp.

BUSES

Hybrid buses: the best or worst of both. Combining two buses on the same backplane offers flexibility, but this technique has not caught on in mainstream systems. Warren Andrews, *RTC*, 5/97, p. 20, 3 pp.

VME64x and CompactPCI: a hybrid approach. Since CompactPCI uses exactly the same mechanics as VME, it is easy to design a backplane that can support both VME and CompactPCI boards. Wayne Fischer, Force Computers; *RTC*, 5/97, p. 26, 2 pp.

Understanding Universal Serial Bus. Part 1: USB basics. Connectivity is a big issue for embedded systems, and the Universal Serial Bus promises to simplify the process. John Canosa, Questra Consulting; *Embedded Systems Programming*, 6/97, p. 34, 14 pp.

DSP

C compilers for DSPs flex their muscles. Before you hand-code your next DSP algorithm, check out the results of the *EDN* compiler benchmark challenge. Markus Levy, *EDN*, 6/5/97, p. 93, 7 pp.

Avoiding design pitfalls in multiprocessor DSP. Overall system performance can be seriously affected if several factors are not addressed in their design. Gord Wait, Spectrum Signal Processing; *Electronic Design*, 5/12/97, p. 95, 4 pp.

IC DESIGN

Core-based design leads the way to flexible system solutions. Multiple design approaches come together at CICC to build high-performance, low-power digital circuits. Dave Bursky, *Electronic Design*, 5/1/97, p. 38, 14 pp.

Not just your basic ASIC libraries. Libraries of basic logic functions, memories, datapaths, and I/O cells are the glue that holds a chip together. Jim Lipman, *EDN*, 6/5/97, p. 52, 6 pp.

BIST's advantages make it a logical choice for more designs. As designs get bigger and more complex, it may not be a question of whether BIST is best, but whether any other methodology will work. John Novellino, *Electronic Design*, 5/12/97, p. 101, 4 pp.

MISCELLANEOUS

The feel of Java. This article provides a firsthand account of some of the design decisions underlying Java and the rationale behind them. James Gosling, Sun; *Computer*, 6/97, p. 53, 5 pp.

Videoconferencing goes to POTS. Because of new standardized codecs, low-cost interoperable products provide toll-quality audio as well as video that ranges from acceptable to very good. Stephen Kempainen, *EDN*, 5/22/97, p. 83, 10 pp.

PC and TV makers battle over convergence. With billions of dollars at stake, computer and TV makers are fighting about whether the digital receivers that will replace the millions of existing analog TVs will be more like PCs or televisions. David Clark, *Computer*, 6/97, p.14, 3 pp.

Videoconferencing is getting better and more affordable. Dedicated chips, high-power microprocessors, and innovative software are making possible high-quality and low-cost computer-based videoconferencing systems. Jules H. Gilder, *Electronic Design*, 5/1/97, p. 89, 8 pp.

PERIPHERALS

MDSL chips lay the cornerstone for cost-effective broadband access. Level One's two-chip multirate DSL data pump (MDP) employs 2B1Q line coding and data scrambling to produce a signal robust enough to carry high-rate data across twisted-pair phone lines for up to 22,000 feet. Lee Goldberg, *Electronic Design*, 5/12/97, p. 54, 2 pp.

Fibre Channel transceiver ups bandwidth, maintains design ease. The Vitesse VSC7214's four independent 8-bit channels allow four times the amount of data to be handled, but at a manageable clock frequency. Richard Nass, *Electronic Design*, 5/12/97, p. 69, 3 pp.

PROCESSORS

Compact-code processor shrinks system memory. LSI's TinyRisc processor uses MIPS-16 to compress code. Bill Jackson, Silicon Graphics; Paul Cobb, LSI; *Electronic Design*, 5/12/97, p. 77, 3 pp.

PROGRAMMABLE LOGIC

Shattering the programmable-logic speed barrier. Upfront planning and careful design, plus an awareness of architecture and development-tool strengths and shortcomings, ensure maximum performance from your programmable-logic device. Brian Dipert, *EDN*, 5/22/97, p. 36, 13 pp.

SYSTEM DESIGN

NiCd: still the popular low-cost battery solution. Despite the falling cost of "greener" and longer-lasting alternatives, NiCd batteries remain prevalent in low-cost, consumer-oriented applications. Stephen Wood, TelAlert; *Electronic Design*, 5/1/97, p. 105, 5 pp.

Provide ESD protection for I/O ports. You can take steps to ensure the safety of some of the most vulnerable components, the interface ICs. Brett Fox and Pirooz Parvarandeh, Maxim Integrated Products; *EDN*, 6/5/97, p. 137, 5 pp.

Use a CPLD to implement an SDRAM controller. SDRAM-controller designs need not be especially difficult; in this design, a CPLD handles the complex aspects. Mark Novak, Mark F. Novak and Associates; *EDN*, 6/5/97, p. 151, 7 pp.