by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,598,553

Program-watchpoint checking using paging with subpage validity
Issued: January 28,1997
Inventors: David E. Richter, et al
Assignee: Exponential Technology
Filed: May 18, 1995
Claims: 25
Segmentation is added to a RISC processor that supports paging. An alternate implementation of Intel-compatible segment-limit checking is shown. Segment-bounds checking is done by comparing the reference to the maximum segment offset in the last page of the segment.

5,598,546

Dual-architecture superscalar pipeline
Issued: January 28, 1997
Inventor: James S. Blomgren
Assignee: Exponential Technology
Filed: August 31, 1994
Claims: 21
A dual-instruction-set processor processes instructions from two or more instruction sets. Instructions are decoded by separate RISC and CISC instruction decoders. A CISC/RISC mode determines which decoder is to decode the instruction. Instructions from several different instruction sets may be mixed in the pipelines.

5,596,733

System for exception recovery using a conditional substitution instruction which inserts a replacement result in the destination of the excepting instruction
Issued: January 21, 1997
Inventors: William S. Worley, Jr., et al
Assignee: HP
Filed: December 22, 1994
Claims: 20
A conditional substitution instruction in an instruction set to correct exceptions occurring during run time. The conditional substitution instruction substitutes a default value for the result of the potentially excepting instruction if the potentially excepting instruction produces any specified exceptions.

5,592,636

Processor architecture supporting multiple speculative branches and trap handling
Issued: January 7, 1997
Inventors: Valeri Popescu, et al
Assignee: Hyundai
Filed: June 6, 1995
Claims: 16
A two-deep branch-prediction system that allows the processor to begin execution of a speculated target-instruction stream that is itself within the target of another speculated target-instruction stream.

5,592,635

Technique for accelerating instruction decoding of instruction sets with variable length opcodes in a pipeline microprocessor
Issued: January 7, 1997
Inventor: Stephen H. Chan
Assignee: Zilog
Filed: July 15, 1994
Claims: 31
In a processor in which instructions are fetched in separate portions by the instruction fetcher, a predecoder decodes first portions of the instruction concurrently with the fetching of the remainder of the instruction.

5,592,634

Zero-cycle multistate branch-cache-prediction data-processing system and method thereof
Issued: January 7, 1997
Inventors: Joseph C. Circello, et al
Assignee: Motorola
Filed: May 6, 1994
Claims: 46
A branch cache comprising entries corresponding to conditional branch instructions, each of which contains the address of the branch, a taken address, a history field, the condition of the branch, and a field used to determine the address that was not taken. The cache allows for conditional branch folding.

5,592,405

Multiple operations employing divided arithmetic-logic unit and multiple flags register
Issued: January 7, 1997
Inventors: Robert J. Gove, et al
Assignee: TI
Filed: June 7, 1995
Claims: 39
A processor that includes an arithmetic-logic unit that is divided into multiple sections. Each section may generate a result representing a combination of respective subsets of its inputs. The arithmetic-logic unit allows for a variety of functions such as add with saturation, maximum pixel transparency, and color expansion. M