by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,613,081

Method of operating a data processor with rapid address comparison for data forwarding
Issued: March 18, 1997
Inventors: Bryan P. Black, et al
Assignee: Motorola
Filed: September 11, 1995
Claims: 15
A forwarding scheme whereby data returning from main memory to a data cache is also forwarded to the processor if the requested data has not crossed a cache-line boundary and the low-order two bits of the requested address match the low-order two bits of the address of the returned data.

5,611,063

Method for executing speculative load instructions in high-performance processors
Issued: March 11, 1997
Inventors: Albert J. Loper, et al
Assignee: IBM
Filed: February 6, 1996
Claims: 11
A method for selectively executing speculative load instructions in a high-performance processor. A speculative load that misses in the cache is performed or not, based on a flag in a table for each load instruction. The flag can be set based on branch history.

5,608,886

Block-based branch prediction using a target-finder array storing target subaddresses
Issued: March 4, 1997
Inventors: James S. Blomgren, et al
Assignee: Exponential
Filed: August 31, 1994
Claims: 21
A branch target-finder array in the instruction cache holds the lower portion of the target address and an encoding indicating whether the target address is within the same 2-Kbyte block as the branch or in the next or previous block. The upper portion of the target address, its block number, is generated by taking the block number of the branch instruction and incrementing and decrementing it or using it as is, depending on the encoding. The target address can be made available at the time the branch instruction is available.

5,611,061

Method and processor for reliably processing interrupt demands in a pipeline processor
Issued: March 11, 1997
Inventor: Hiroyuki Yasuda
Assignee: Sony
Filed: November 24, 1993
Claims: 5
Method and system for taking interrupts in a pipelined processor. In a first cycle, the processor recognizes an interrupt at the end of the execution of a first instruction and while fetching a second. In a second cycle, a third instruction is fetched and pushed. In a third cycle, the address of the second instruction is pushed while the first instruction of the ISR is fetched. Unwinding is done at the end of the ISR.

5,608,892

Active cache for a microprocessor
Issued: March 4, 1997
Inventor: John F. Wakerly
Assignee: Alantec
Filed: June 9, 1995
Claims: 3
A cache is external to a microprocessor and forms a second-level cache that is novel in its ability to perform transfers from external random-access memory independently of the microprocessor. The cache also provides the ability to encache misaligned references and to transfer data to the microprocessor in bursts.

5,608,885

Method for handling instructions from a branch prior to instruction decoding in a computer that executes variable-length instructions
Issued: March 4, 1997
Inventors: Ashwani K. Gupta, et al
Assignee: Intel
Filed: March 1, 1994
Claims: 3
A circuit and method for fetching and rotating variable-length macroinstructions to an instruction buffer for an instruction decoder that receives and decodes multiple macroinstructions in parallel.

OTHER ISSUED PATENTS

5,613,080 *Multiple execution-unit dispatch with instruction shifting between first and second instruction buffers based upon data dependency*
5,612,911 *Circuit and method for correction of a linear address during 16-bit addressing*
5,611,071 *Split replacement cycles for sectored cache lines in a 64-bit microprocessor interfaced to a 32-bit bus architecture* M