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The IA-64 instruction set melds features from RISC and VLIW into a new style called EPIC—explicitly parallel instruction computing—that should give Merced an architectural performance advantage.	
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A look back at the 21164, PA-8000, R10000, PowerPC 620, and UltraSparc provides insight into which strategies succeeded.	
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Intel, Digital attempt settlement; BOPS raises curtain on ManArray DSP; S3 integrates DRAM with notebook 3D; Corollary acquisition boosts Intel server plans; LPC offers low-cost ISA replacement.	
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IBM, Moto write embedded PowerPC plans; Rockwell unearths Java JEM; AMD pushes Elan to 100 MHz; NEC R4310 upgrades R4300 to 167 MHz; IDT inaugurates integrated MIPS with 36100; RM5270 is fastest QED processor; SuperH chips get FPU, 100-MHz upgrade; Pentium/MMX gets plastic PGA for embedded.	
M•Core Shrinks Code, Power Budgets	12
Motorola's newest 32-bit instruction set is aimed at low-cost, low-power applications that ColdFire and PowerPC can't reach.	
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The N7 combines a low-end Pentium-class CPU with enough system logic to build a complete PC—or NC—on a single chip.	
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The K6 will gain a 100-MHz bus and a faster MMX unit early next year, along with a set of new FP instructions to speed 3D programs.	
Cayenne Spices Up Cyrix's 6x86MX	22
Cyrix's next CPU gains improved FP and MMX performance along with a set of new FP instructions to speed 3D programs.	
Direct RDRAM Sustains 1.5 Gbytes/s	25
The new Rambus interface uses an 18-bit data bus and a separate command bus to deliver sustained bandwidth of nearly 1.5 Gbytes/s.	
UltraSparc-3 Aims at MP Servers	29
Due in early 1999, Sun's next processor hits 600 MHz, and its unusual four-bus design provides more than 20 Gbytes/s of total bandwidth—ideal for systems with large numbers of processors.	
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With several x86 vendors providing incompatible instruction-set extensions for 3D programs, the x86 market is fragmenting.	
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