IBM, Moto Write Embedded PowerPC Plans

Unifying their embedded efforts, PowerPC partners IBM and Motorola are writing a new specification for embedded PowerPC chips, and they will open up licensing to interested third parties. The first chips to result from this plan are not expected for more than a year.

The heart of the agreement is Book E, a new document that spells out how future embedded PowerPC chips will be designed. Book E is divided into five sections: the user-mode instruction set; memory management; protection mechanisms; a 16/32-bit code-compression mechanism; and new 32-bit extensions for media- and signal-processing. Section 1 is equivalent to the current "Book 1" definition of the instruction set that all PowerPC chips adhere to today.

IBM and Motorola will still compete with each other in the embedded market, as they do today; Book E doesn't change that. The purpose of Book E is to prevent the two vendors from developing incompatible versions of the same feature. For example, it would prevent Motorola and IBM from designing mutually incompatible multiply-accumulate instructions, as some of the MIPS vendors have done. Book E does not, however, prevent either party from adopting its own application-specific extensions to the PowerPC architecture without the consent of the other party.

The most interesting part of Book E will be the last two sections. Until now, neither of the PowerPC partners has discussed any plans for media extensions or for code compression, both of which are becoming common features among PowerPC's competitors. (There are rumors of VMX extensions in future G4 desktop chips.) Both parties admit that work in both areas is just beginning, so a fixed definition of these extensions—much less chips that implement them—is still many months away.

Which chip vendors might license PowerPC isn't clear. As part of the agreement, both IBM and Motorola revealed that they are not in "serious negotiations" with any potential licensees at this time, so an immediate licensing deal doesn't appear to be imminent. The companies cited requests from certain high-volume customers with their own fabs, who might wish to hold a license as a hedge against production problems or as a lever in times of shortage. Such licensing deals are likely to be made quietly if they happen.

Looking ahead, it's encouraging to see both Motorola and IBM take positive steps toward making PowerPC a more powerful force in the embedded market. With the ink not yet dry on the agreement, however, it will likely be more than a year before anything tangible comes of it. —*J.T.*

Rockwell Unearths Java JEM

Seemingly out of nowhere, Rockwell Avionics and Communications has developed its own processor that directly executes Java bytecodes. Paradoxically, even though Rockwell is a licensee of Sun's PicoJava 1 core (see MPR 10/28/96, p. 28), Rockwell did not use PicoJava. Instead, the Iowa-based company dusted off an internal stack-based design that it developed nearly 15 years ago. After some significant alterations, the new chip, dubbed JEM1, executes Java bytecodes as its native instruction set.

In a possible foreshadowing of Java processors' future, Rockwell stated it is uncertain what customers there may be for JEM1. The company felt that, given its background, avionics might be one possibility, adding that the chip should not be used in "flight-critical" applications. Rockwell is currently negotiating with Sun Microelectronics to offer JEM1 on the open market.

The chip is entirely microcoded. Rockwell engineers replaced the microcode for the original AAMP (advanced-architecture microprocessor) instruction set with new microcode for bytecode interpretation. The CPU core, including 2K of microcode ROM, measures 2×3 mm in a 0.5-micron CMOS process. This size is much smaller than the PicoJava 1 core, which Sun estimates at 8 mm^2 in a 0.35-micron process. JEM1 executes virtually all Java bytecodes directly in hardware, with only 2–3 pathological cases handled through software libraries. This is in contrast to PicoJava 1, which emulates about 20% of the defined bytecodes.

In military temperature ranges, JEM1 is qualified for 50-MHz operation. In commercial temperatures, Rockwell believes 65–70 MHz is attainable. Rockwell has not set pricing for the JEM1; the part is sampling now, but production schedules have not been set.

Rockwell intends to move ahead with PicoJava-based chips in addition to its internally developed designs. The company plans to offer both families and let its customers decide which they prefer. —*J.T.*

AMD Pushes Elan to 100 MHz

Owing to yield improvements, AMD has pushed the speed of its two 486-based Elan devices (see MPR 10/28/96, p. 4) to 100 MHz. The faster Elan 400 and Elan 410 are available immediately at $55.65 and $51.33 in 10,000-unit quantities, respectively.

Since introducing its 486-based Elan chips in 1996, AMD has enjoyed a surge of interest from customers who initially shied away from Elan. Integrated x86 devices in general have enjoyed mixed success, and customers were wary of being stranded with a dead-end part. Now, with a pair of 386-based chips and a compatible pair of 486-based chips, interest in Elan as a whole has waxed. At more than $50 for a 100-MHz 486, Elan won't take home any price/performance trophies, but the ability to embed a PC in just four square inches is nonetheless attractive to a number of embedded customers. —*J.T.*

NEC R4310 Upgrades R4300 to 167 MHz

NEC has increased the speed of its successful R4300 processor, used in games, printers, and network boxes. The new chip runs at 167 MHz, a 25% speed increase over the previous 133-MHz limit.

To reach the new speed, NEC moved the part onto its 0.28-micron CMOS process (the R4300 is built on a 0.35-micron line). The new process shrinks the size of the R4300 die and reduces the chip's power consumption. To honor the changes, NEC has rechristened the faster part R4310.

Pricing for the 167-MHz R4310 is the same as the previous price for the 133-MHz R4300: $25 in 10,000-piece quantities. This suggests that NEC will soon drop the price of the R4300 to about $20. Despite the process shrink, the R4310 still uses a single 3.3-V power supply for core and I/O. The R4310 is pin-compatible with the R4300; to accommodate the faster internal clock speed without altering bus timing, the R4310 supports additional clock divisors.

Sampling of the R4310 has already begun; production volumes are expected in 2Q98. With the advent of the new part, prices for the R4300 will likely drop rapidly, pushing them closer to those of NEC's R41xx parts (see MPR 10/6/97, p. 13). With a number of high-performance parts clustered around the $20–$25 price range, NEC will probably rapidly discontinue the older devices. We expect the company will then start on a family of integrated chips based on the R4300/4310 core that address specific markets and raise NEC's average selling price. —*J.T.*

IDT Inaugurates Integrated MIPS with 36100

As the first of a promised line of low-end integrated MIPS chips, IDT has rolled out its 36100, a 33-MHz part with peripherals for serial-data transmission.

The 36100 (not to be confused with Philips' 31700) includes an R3000 CPU core, 4K/1K of instruction/data cache, a memory controller, timers, parallel I/O, and two intelligent serial-communications channels. In 10,000-piece lots, the 36100 is priced at $38, $42, and $45 in 20-, 25-, and 33-MHz speed grades, respectively. All three versions are available now in a 208-lead metal QFP.

Integration is becoming more important than performance for many customers and an important differentiating factor for a vendor. An integrated chip carries more value than its silicon area might otherwise suggest. On the other hand, integrated devices are almost universally sole-sourced, making customers nervous. They also lose their value when application demands change, or if the part was not well-specified to begin with. IDT seems willing to take that gamble, with a number of new integrated MIPS-based devices set to roll out in the next 12 months. —*J.T.*

RM5270 Is Fastest QED Processor

The elves in QED's hollow tree have craftily fashioned another MIPS processor in that company's line of fast embedded CPUs. The new RM5270 is the fastest part yet in QED's line, holding a position between the existing RM5260 and the forthcoming RM7000.

Internally, the RM5270 is like its siblings, the RM5230 and RM5260, with an R5000-derived core, dual 16K caches, an FPU, and multiply-accumulate extensions. The chip also includes cache-locking and interrupt-response tweaks that make it desirable for embedded applications. Externally, the new RM5270 adds an L2 cache controller and a faster, 100-MHz system bus.

Another significant feature of the RM5270 is that it is pin-compatible with the much-delayed RM7000. Thus, the RM5270 can be used as a stopgap until the RM7000 arrives (currently scheduled for 1Q98). QED rates the new part at 5.0 SPECint95 and 5.2 SPECfp95, or 260 MIPS using the more pedestrian Dhrystone 2.1 benchmark.

Priced at $75 for 150 MHz and $100 for 200 MHz, the RM5270 is significantly more expensive than either the RM5230 or RM5270. But with an L2 cache controller and a fast, wide bus interface, the chip is significantly more powerful as well. More important, the RM5270 is positioned as an RM7000 upgrade waiting to happen, so it is more likely to appeal to workstation-level customers than traditional embedded users. —*J.T.*

SuperH Chips Get FPU, 100-MHz Upgrade

Hitachi has significantly boosted the speed of its SH7708 processor from 60 MHz to 100 MHz and introduced the SH7718, the first SuperH part with a floating-point unit. Both chips will begin sampling in December, with production slated for 1Q98. The new SH7708 will sell for $21; the SH7718 is priced at $25—both in 100-MHz speed grades, in quantities of 10,000 units.

The SH7718 is based on the SH-3E core design (see MPR 12/4/95, p. 10), an enhancement to the SH-3 core used in several existing parts. The SH-3E adds single-precision floating-point instructions by extending the instruction word to 32 bits and adding eight new FP registers. The FP extensions are incompatible with the DSP extensions embodied in the SH7410 (see MPR 3/31/97, p. 4). Hitachi expects the FP-equipped SH7718 will appeal mainly to designers who want more accurate graphics rendering (i.e., for laser printers) or who focus on motion control. —*J.T.*

Pentium/MMX Gets Plastic PGA for Embedded

Intel has repackaged its 200-MHz Pentium/MMX in a plastic pin-grid array (PGA) for use in embedded systems. At $252, the chip is priced the same as the normal desktop version.

Intel also rolled out a 166-MHz Pentium/MMX module (see MPR 6/23/97, p. 10), topping the previous 133-MHz non-MMX offering. Sampling in 1Q98, the module will be priced at $400. Although neither of these processors is new, Intel's move is significant because it signals the start of long-term availability for these particular versions, a guarantee that many embedded designers need. —*J.T.*