by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,625,837

Processor architecture having out-of-order execution, speculative branching, and giving priority to instructions which affect a condition code
Issued: April 29, 1997
Inventors: Valeri Popescu, et al
Assignee: Hyundai
Filed: June 6, 1995
Claims: 5
An out-of-order data processor assigns a priority to instructions in a reservation station. Instructions that set condition codes are given a higher priority so that branch predictions can be confirmed earlier than they would be otherwise.

5,625,835

Method and apparatus for reordering memory operations in a superscalar or very-long-instruction-word processor
Issued: April 29, 1997
Inventors: Mahmut K. Ebcioglu, et al
Assignee: IBM
Filed: May 10, 1995
Claims: 3
Method and design for processing load instructions speculatively in an out-of-order superscalar or VLIW processor. The method checks for exceptions generated by speculatively performing a load. If exceptions are generated, a delayed exception bit is associated with the register targeted for the loaded data. If an exception would not be generated, the load is performed to a rename register. All subsequent in-order stores are compared with the load address. If no store overwrites the location, the load is committed in order.

5,625,808

Read-only store as part of cache store for storing frequently used millicode instructions
Issued: April 29, 1997
Inventors: Charles F. Webb, et al
Assignee: IBM
Filed: May 31, 1995
Claims: 6
A method by which vertical microcode (i.e., millicode) can be patched. Entry points to the microinstruction sequences have an associated register that directs the millicode fetcher either to the read-only microcode or to an alternate entry point in main memory.

5,625,806

Self-configuring speed path in a microprocessor with multiple clock option
Issued: April 29, 1997
Inventor: Stephen C. Kromer
Assignee: AMD
Filed: August 8, 1996
Claims: 8
A microprocessor that reconfigures its internal critical paths based on an external selection of its operating frequency. Critical-path hardware is reconfigured to take multiple clocks when a high operating frequency is chosen and a single clock when a lower operating frequency is chosen.

5,625,793

Automatic cache bypass for instructions exhibiting poor cache hit ratio
Issued: April 29, 1997
Inventor: Jamshed H. Mirza
Assignee: IBM
Filed: April 15, 1991
Claims: 11
A computer system that adjusts the cachability of a line in the cache based on the number of misses to that line.

5,625,789

Apparatus for source operand dependency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle
Issued: April 29, 1997
Inventors: James H. Hesson, et al
Assignee: IBM
Filed: October 24, 1994
Claims: 5
A pipelined out-of-order superscalar microprocessor that has a rapid recovery from branch-prediction misses. Loads and stores are permitted out of order.

5,625,788

Microprocessor with novel instruction for signaling event occurrence and for providing event-handling information in response thereto
Issued: April 29, 1997
Inventors: Darryl D. Boggs, et al
Assignee: Intel
Filed: March 1, 1994
Claims: 16
In an out-of-order microprocessor, a method and apparatus for signaling the occurrence of an event via a microinstruction issued to an execution unit when the condition that would generate the event is detected. M