Hennessy & Patterson, Rev 2.0

Microprocessor design demigods David Patterson and John Hennessy, along with their publisher Morgan Kaufmann, have just released *Computer Organization & Design*, Second Edition. With more than 950 pages, this "introduction to the field" is comprehensive in its scope and methodical in its approach. Pipelines, instruction sets, memory hierarchies, and other subjects are all developed here, using the MIPS architecture as a working example.

Copies can be ordered from the publisher (San Francisco) for \$79 by calling 800.745.7273 or visiting www.mkp.com.

Supercomputers Heat Up San Jose

The IEEE/ACM supercomputer fest, SC97, rolls into the San Jose (Calif.) Convention Center November 15–21. The week will be filled with a combination of tutorials, papers, award sessions, and exhibits. Talks will include "High-Performance Data Mining," "Shared Memory Parallel Programming," "A Practical Guide to Java," the compelling "Implementation Methods for Parallel Adaptive Mesh Refinement Solutions of Partial Differential Equations," and the curiously titled, "How to Build a Beowulf: Assembling... a Do-It-Yourself Supercomputer."

Registration fees range from \$100 to \$910, depending on number of days/events attended and IEEE membership status. For more information, see www.supercomp.org/sc97.

MICRODESIGN RESOURCES

NEW TECHNICAL LIBRARY REPORTS

Beyond Conventional 3DTalisman and Other Advanced Architectures

Peter Glaskowsky, MDR's 3D and multimedia specialist, explains how Microsoft's Talisman and other advanced architectures will redefine the conventional 3D pipeline. The report offers an insightful exploration of the dangers and opportunities this conversion offers to 3D hardware and software vendors while pointing out which companies have the edge in this transition.

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Intel's Merced and IA-64 Technology and Market Forecast

Intel expert Linley Gwennap explains why Intel is developing a new instruction set and analyzes the key features that were recently revealed. The report examines the impact IA-64 will have on PC makers, workstation and server vendors, and Intel's competitors. You'll also find MDR's forecast of key parameters such as clock speed, die size, and performance for Merced and its successors. *Release Date: 11/97*

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The Wescon IC Expo will fill the San Jose (Calif.) and Santa Clara Convention Centers November 4–6, promising three days of "The Largest Technology Event in Silicon Valley." Talks and tutorials will pander to the tastes of engineers, purchasing managers, distributors, manufacturers, and business professionals. And it's free, too. For more information, contact Wescon (Los Angeles) at 800.877.2668 or set your browser to www.wescon.com.

Digital Camera Sales to Zoom

So say Future Image and IDC, joint authors and publishers of *Digital Camera Market Forecast and Analysis, 1996–2001*. The report estimates overall sales of digital cameras will exceed \$4 billion by 2001. Digital cameras priced from \$99 to \$45,000 are considered in the unit and revenue forecasts, as are all the current and expected market players. Copies of the report cost \$5,000. For more information, call Future Image (Burlingame, Calif.) at 650.579.0566 or check out *www.futureimage.com*.

Sparse Matrix Kernels for Shared Memory

Carnegie Mellon scientist David O'Hallaron's "kernels for core sparse matrix-vector product operation from finite element simulations" are at www.cs.cmu.edu/~quake/spark98.html. These portable kernels are ideal for testing or benchmarking systems for large-data-set applications.

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