AUDIO/VIDEO

Know the design issues in achieving consumer-quality video for PCs. The right mix of hardware and software splits open bottlenecks and produces high-quality video for entertainment PCs. Hemant Bheda, Mediamatics; *Electronic Design*, 11/97, p. 57, 6 pp.

BUSES

CPCI passes potholes, enters the on-ramp. CompactPCI, a blend of VME and desktop-PC technology, holds promise as an industrial computer bus. A growing mass of products is making that promise a reality. Richard A. Quinnell, *EDN*, 10/97, p. 91, 7 pp.

A tale of three buses: DeviceNet, Profibus-DP, Foundation Fieldbus. The best of buses for one industrial-automation application can be the worst of buses for another. Mike Santori, National Instruments; *EDN*, 10/97, p. 149, 7 pp.

Serial bus technologies stake out territories. Fiber channel, 1394 (FireWire), and USB have burst onto the scene as mainstream technologies. Together, the buses form a continuum of serial connectivity for microprocessor-based systems. Jeff Child, *Computer Design*, 11/97, p. 102, 4 pp.

Ring architecture connects up to 128 PCI buses. Single-chip interface allows dual rings to add fault tolerance without dropping PCI compatibility. Richard Nass, National Instruments; *Electronic Design*, 11/97, p. 85, 3 pp.

DSPS

Modem technologies: the choice is yours. The 56-kbps wars may garner the headlines, but the real excitement in modems lies in the hardware design. Chip sets are still the first choice, but host-based implementations are closing in quickly. Maury Wright, *EDN*, 11/97, p. 48, 8 pp.

IC DESIGN

Readers speak out on deep submicron. An RTL interoperability standard, floorplanning, and placement is needed. Jonah McLeod, *Integrated System Design*, 11/97, p. 16, 5 pp.

Deep-submicron designs require netlist reduction for fast simulation. Hitachi uses a new tool to reduce cache memory megacell netlists to a manageable size. Jack S. Thomas, Hitachi Micro Systems, et al; *Integrated System Design*, 11/97, p. 40, 4 pp.

MISCELLANEOUS

Windows CE—What's in it for you? Microsoft is starting to take the embedded systems market seriously. Larry Mittag, Stellcom Technologies; *Embedded Systems Programming*, 11/97, p. 20, 5 pp.

PERIPHERALS

LAN/WAN interfaces: plugging into the cloud. Today's distributed organizations rely on a web of T1, ISDN, and ATM to tie their branch and home offices together. This has created a huge market for chips, boards, and boxes that bridge the LAN/WAN gap. Lee Goldberg, Stellcom Technologies; *Electronic Design*, 11/97, p. 109, 6 pp.

PROCESSORS

General-purpose µPs for DSP applications: consider the trade-offs. General-purpose processors instead of dedicated DSPs are a viable option in some system designs. Garrick Blalock, Berkeley Design Technology; *EDN*, 10/97, p. 165, 5 pp.

Two fast and high-associativity cache schemes. Parallel and sequential multicolumn cache schemes increase associativity while keeping cycle times low. Chenxi Zhang, Changsha Institute of Technology, et al; *IEEE Micro*, 9–10/97, p. 40, 10 pp.

Superscalar instruction issue. Design space (DS) trees can help to concisely represent the design space of instruction issue. Dezsõ Sima, Kandó Polytechnic, Budapest; *IEEE Micro*, 9–10/97, p. 28, 11 pp.

Exploiting instruction- and data-level parallelism. Simultaneous multithreaded vector architectures combine the best of data-level and instruction-level parallelism and perform better than either approach could separately. Roger Espasa and Mateo Valero, Polytechnic University of Catalunya-Barcelona; *IEEE Micro*, 9–10/97, p. 20, 7 pp.

Simultaneous multithreading: a platform for next-generation processors. Simultaneous multithreading exploits both instruction-level and thread-level parallelism by issuing instructions from different threads in the same cycle. Susan J. Eggers, University of Washington, et al; *IEEE Micro*, 9–10/97, p. 12, 7 pp.

Asynchronous processor survey. A look at several experimental approaches indicates that asynchronous processors may one day offer improvements over present system performance. Tony Werner and Venkatesh Akella, University of California, Davis; *Computer*, 11/97, p. 67, 9 pp.

PROGRAMMABLE LOGIC

New programmable logic devices address modern designs. Better software and new logic architectures are changing design decisions for engineers. Peter Varhol, *Computer Design*, 11/97, p. 64, 4 pp.

FPGAs pack distributed SRAM and flexible logic. Small blocks of SRAM and eight-way logic cell connectivity combine to give FPGAs more flexibility. Dave Bursky, *Electronic Design*, 11/97, p. 46, 2 pp.

SYSTEM DESIGN

Integrating IP blocks to create a system-on-a-chip. When faced with system ASIC design, take inventory of your resources before selecting an ASIC vendor, foundry, or design-services provider as your partner. Consider emerging standards and choose design methodologies that will ease IP integration. Barbara Tuck, *Computer Design*, 11/97, p. 49, 9 pp.

System management mode offloads overworked 8259 interrupt controller. This article explains how SMI (system management interrupt) works. Jim Kelsey, SystemSoft; *Personal Engineering & Instrumentation News*, 11/97, p. 47, 4 pp.