by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,630,149

Pipelined processor with register-renaming hardware to accommodate multiple-size registers
Issued: May 13, 1997
Inventor: Mark Bluhm
Assignee: Cyrix
Filed: November 20, 1995
Claims: 16
Register renaming in a microprocessor where physical registers are allocated to logical registers based on the size of the logical register.

5,630,143

Microprocessor with externally controllable power management
Issued: May 13, 1997
Inventors: Robert Maher, et al
Assignee: Cyrix
Filed: September 22, 1994
Claims: 14
A microprocessor with circuitry that detects an external control signal and disables the clock signals to one or more of the subcircuits of the processor.

5,630,097

Enhanced cache operation with remapping of pages for optimizing data relocation from addresses causing cache misses
Issued: May 13, 1997
Inventors: David A. Orbits, et al
Assignee: Digital
Filed: January 7, 1994
Claims: 18
A computer system with virtual memory having a cache that reduces misses by remapping pages of physical memory when cache misses are detected by changing the page tables.

5,630,095

Method for use with a data-coherency protocol allowing multiple snoop queries to a single snoop transaction and system therefore
Issued: May 13, 1997
Inventor: Michael D. Snyder
Assignee: Motorola
Filed: July 3, 1995
Claims: 2
A snoop method and apparatus in a processor which operates at at least 2× the bus clock. The system interrogates the internal caches for each internal cycle until the caches are not busy or the next bus cycle occurs. Either busy or the snoop result is then delivered.

5,630,082

Apparatus and method for instruction-queue scanning
Issued: May 15, 1997
Inventors: Nathan L. Yao, et al
Assignee: AMD
Filed: August 18, 1994
Claims: 24
In a superscalar CISC processor, an instruction decoder that marks instruction boundaries and predecodes the CISC instructions into RISC instructions (ROPS).

5,630,075

Write-combining buffer for sequentially addressed partial-line operations originating from a single instruction
Issued: May 13, 1997
Inventors: Mandar S. Joshi, et al
Assignee: Intel
Filed: May 25, 1995
Claims: 34
A write-combining buffer in a microprocessor that buffers writes to memory at nearby addresses so the physical memory writes can be done on a larger granularity than the individual writes. The buffer includes an address tag, validity bits on a byte basis, and a data portion.

5,630,146

Method and apparatus for invalidating a cache while in a low-power state
Issued: May 13, 1997
Inventors: James W. Conary, et al
Assignee: Intel
Filed: October 16, 1995
Claims: 18
Method and apparatus allow a processor to invalidate an individual line of its cache while in a nonclocked low-power state.

5,630,083

Decoder for decoding multiple instructions in parallel
Issued: May 13, 1997
Inventors: Adrian L. Carbine, et al
Assignee: Intel
Filed: July 3, 1996
Claims: 15
A decoder for decoding instructions in parallel, including a full decoder that decodes an instruction into multiple micro-operations, and (a) partial decoder(s) that can decode a subset of the instructions. M