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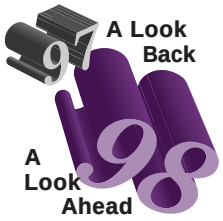
Slot vs. Socket Battle Heats Up

Intel Prepares for Transition as Competitors Boost Socket 7



by Michael Slater

The past year has brought a great deal of change to the x86 microprocessor market, with Intel, AMD, and Cyrix replacing virtually their entire product lines with new devices. But despite high hopes, AMD and Cyrix struggled in vain for profits. The financial contrast is stark: in 1997, Intel earned a record $6.9 billion in net profit, while AMD lost $21 million for the year and Cyrix lost $6 million in the six months before it was acquired by National. New entrant IDT added another competitor to the mix but hasn't shipped enough products to become a significant force.

MMX swept the market with startling speed. Beginning with the Pentium/MMX introduction in early January, followed by AMD's K6 in the spring and Cyrix's 6x86MX in early summer, MMX processors swiftly took over the market and pushed the remaining non-MMX chips into the bargain bin. Intel's aggressive pricing was a driving factor: after initially charging a steep premium for Pentium/MMX, Intel slashed prices midyear (see MPR 1/26/98, p. 31 for pricing details).

The coming year promises no less change. In 1997, Intel offered Pentium II (Slot 1) processors predominantly for midrange and high-end systems, in large part because it lacked the manufacturing capacity to move the large die into the highest-volume parts of the market. In 1998, a die shrink and increased capacity will enable Intel to drive Pentium II into entry-level systems, making life considerably more challenging for the alternative vendors and their Socket 7 (Pentium pin-compatible) processors. While only about 15% of the roughly 80 million processors Intel shipped in 1997 were Pentium IIs or Pentium Pros, Pentium II will dominate Intel's shipments by the second half of 1998.

Production limits were the biggest factor holding back Intel's competitors in 1997. AMD and Cyrix were unable to ship as many parts as they hoped, especially at the highest clock speeds where profits are much greater.

The shift to 0.25-micron technology will be central to 1998's CPU developments. Intel began shipping 0.25-micron processors in 3Q97; AMD followed late in 1997, IDT plans to join in by mid-98, and Cyrix expects to catch up in 3Q98. The more advanced process technology will cut power consumption, allowing sixth-generation CPUs to be used in notebook systems. The smaller die sizes will enable higher production volumes and make it possible to integrate an L2 cache on the CPU chip.

The processors from Intel's challengers have lagged in floating-point and MMX performance, which the vendors plan to fix in 1998. They also will add 3D instruction-set extensions, pulling ahead of Intel in that respect.

In terms of CPU cores, 1998 will be a year of incremental enhancements. Much of the change will be in bus interfaces and cache strategies, as Figure 1 shows. Most of Intel's

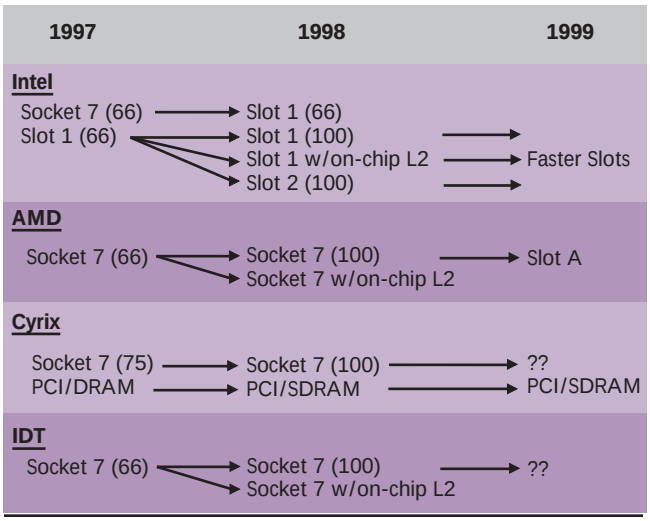


Figure 1. While Intel seeks to shift the market to Slot 1 and Slot 2 this year, Intel's competitors will boost Socket 7 to 100 MHz. All but Cyrix will add on-chip L2 cache. (Bus speed in parenthesis)

new products will be various modules based upon the just introduced Deschutes version of Pentium II. AMD, Cyrix, and IDT will all introduce processors based on enhanced versions of the chips they are shipping today—though in some cases the enhancements are significant. Table 1 summarizes the new lineup.

MMX Not the Key Force Behind MMX Success

While it is tempting to consider the sweeping MMX transition a great endorsement for MMX technology, the new instructions themselves had little to do with the shift. Only a handful of application types gain compelling benefit from MMX, and MMX is nearly irrelevant to typical business users. The most popular application that greatly benefits from MMX is image editing, which is becoming increasingly important with the surge in digital photography but is still far from a mainstream application.

Through tens of millions of dollars in advertising, complete with the now infamous bunny people, Intel succeeded in creating demand for MMX that had little to do with the immediate value of the technology. For the first time, microprocessor advertising reached true consumer levels, where products are sold on emotional appeal without letting any actual information get in the way.

With larger on-chip caches, higher clock speeds, and lower power consumption, the Pentium/MMX, K6, and 6x86MX designs are superior to their predecessors even without any software that uses MMX. This factor, combined with consumers' fear of buying an obsolete processor, drove the rapid transition to MMX.

Now that the installed base of MMX systems is in the tens of millions and nearly all new systems have MMX, software developers will give more consideration to MMX. Its use in application code will remain limited, but more system functions—such as soft modems, MPEG-2 decoders, video-conferencing codecs, and audio codecs—will use MMX and thereby lighten the load they place on the CPU.

Beyond MMX: New Instructions Accelerate 3D

Despite the existence of a few 3D games that use MMX to accelerate rendering, as well as an MMX-optimized software renderer in Direct3D, the new instructions aren't useful for 3D in the long run. Once a system has 3D rendering hardware, which is the case today for all consumer systems except the least expensive ones, rendering—the only part of the 3D pipeline where MMX is useful—is handled by the graphics accelerator.

The geometry and lighting portions of the 3D pipeline are likely to remain host-based for most users, however, and there is a great opportunity to increase the CPU's performance on these tasks with further instruction-set extensions. Just as MMX provides SIMD (single instruction, multiple data) support for integer data, new extensions will do the same for floating-point data, which is typically used in 3D geometry calculations. By storing two single-precision FP values in a single 64-bit register and operating on both in parallel, FP throughput can be doubled. Furthermore, by using direct register addressing, the new instructions can bypass the clumsy stack structure of the standard x86 floating-point unit.

At last October's Microprocessor Forum, AMD, Cyrix, and IDT all revealed plans to implement such extensions—but each vendor took a different, incompatible approach, and each added different instructions beyond SIMD floating point. The vendors were unaware of the others' efforts before the Forum, as each had been afraid to talk to the others for competitive reasons. Discussions about converging on a standard began at the Forum, and with encouragement from Microsoft, the three companies agreed to rally around a single set of instructions—although a formal agreement has not been announced as of this writing. The technical issues

Vendor & family	Code name	Bus interface	Max. bus speed	L1 cache (I/D)	L2 cache	L2 speed	3D ext.	Max clock speed	First avail.§	Process*	Die size*	Est. mfg cost†
Intel	P55C	Socket 7	66 MHz	16K/16K	external	bus speed	no	233 MHz	1Q97	0.35µ 3M	128 mm²	$55
Pentium/MMX	Tillamook	Socket 7	66 MHz	16K/16K	external	bus speed	no	266 MHz	3Q97	0.25µ 4M	98 mm²	$45
Intel	Klamath	Slot 1	66 MHz	16K/16K	512K	1/2 CPU	no	300 MHz	2Q97	0.35µ 4M	203 mm²	$105
Pentium II	Deschutes	Slot 1	100 MHz	16K/16K	512K	1/2 CPU	no	450 MHz	1Q98	0.25µ 4M	131 mm²	$85
	Deschutes	Slot 2	100 MHz	16K/16K	1M+	CPU speed	no	450 MHz	2Q98	0.25µ 4M	131 mm²	$185
	Covington	Slot 1	66 MHz†	16K/16K†	none	none	no	266 MHz†	3Q98	0.25µ 4M	131 mm²	$70
	Mendocino	Slot 1	100 MHz†	16K/16K†	256K on-chip	CPU speed	no	450 MHz†	4Q98	0.25µ 4M	160 mm²†	$80
AMD	K6	Socket 7	100 MHz	32K/32K	external	bus speed	no	300 MHz	1Q98	0.25µ 5M	68 mm²	$45
K6	K6 3D	Socket 7	100 MHz	32K/32K	external	bus speed	yes	350 MHz	2Q98	0.25µ 5M	81 mm²	$50
	K6+ 3D	Socket 7	100 MHz	32K/32K	256K on-chip	CPU speed	yes	400 MHz	2H98	0.25µ 5M	135 mm²	$60
Cyrix	MediaGX/MMX	PCI/DRAM	33/100 MHz	16K unified	none	none	no	300 MHz	1Q98	0.35µ 4M	142 mm²	$45
	6x86MX	Socket 7	100 MHz	64K unified	external	bus speed	no	PR350	2Q97	0.25µ 5M	69 mm²	$40
	MXi	PCI/DRAM	33/133 MHz	64K unified	none	none	yes	350 MHz	2H98	0.25µ 5M	90 mm²	$55
	Cayenne	N.D.	N.D.	64K unified	N.D.	N.D.	yes	PR350	2H98	0.25µ 5M	70 mm²	$45
IDT	C6	Socket 7	75 MHz	32K/32K	external	bus speed	no	240 MHz	4Q97	0.35µ 3M	88 mm²	$40
WinChip	C6+	Socket 7	100 MHz	32K/32K	external	bus speed	yes	300+ MHz	2Q98	0.25µ 3M	58 mm²	$35
	C6+ L2	Socket 7	100 MHz	32K/32K	256K on-chip	CPU speed	yes	300+ MHz	2H98	0.25µ 3M	110 mm²†	$45

Table 1. In 1998, Intel will proliferate its Pentium II design to higher and lower price points, while its competitors enhance their Socket 7 offerings. N.D. = not disclosed *for most advanced version §for process version listed (Source: vendors except †MDR estimates)

appear to be settled, with marketing concerns holding up the announcement.

The converged instruction set will implement the common subset of the extensions defined by AMD and Cyrix. Because AMD was the furthest along (it has working silicon and early versions of 3D acceleration software running), Cyrix agreed to use AMD's opcodes. Each vendor will drop some instructions that were not in the other's definition.

In early 1999, Intel will introduce its own set of 70 new 3D acceleration instructions with the processor code-named Katmai. Although press reports have called these instructions MMX2, Intel does not use this name; Intel refers to them simply as "Katmai new instructions." Intel says it is working with hundreds of software developers and will ship development systems to these companies in mid-1998.

AMD expects to ship processors with its 3D extensions in the second quarter, putting it more than six months ahead of Intel. IDT expects to ship its C6+, with the 3D extensions, by midyear, lagging AMD by only a month or so. Cyrix will trail AMD and IDT in shipping processors with the 3D extensions but should still beat Intel to market.

The AMD/Cyrix/IDT extensions will be supported in Direct3D version 6, due from Microsoft in 2Q98, so games that use Direct3D for geometry and lighting (G&L) will benefit automatically. Most games still use proprietary G&L code, and some game developers will offer versions of these games with G&L code optimized for the new instructions.

Intel is no doubt working hard to convince game developers to focus on Katmai instead. Because Intel won't have this chip ready for Christmas 1998, however, and because the game community is accustomed to supporting special hardware for a performance boost, there is a good chance Intel's competitors will have enough software that uses their extensions to make their chips more attractive than ever for 3D game enthusiasts. Going into the 1998 Christmas season, this could give Intel's competitors their biggest advantage ever.

In 1999, however, the focus will swing back to Intel; the Katmai new instructions are likely to include more capabilities than the competitors' design and to be more widely supported. By the end of 1999, even the chips from Intel's competitors probably will support the Katmai new instructions. The competitors will continue to support their alternative extensions as well, although possible conflicts in assigning opcodes could create problems.

Cache and Bus Strategies at the Forefront

Aside from instruction-set extensions, the biggest shifts will be in cache and bus strategies. So far, Intel's Pentium II is the only x86 processor (other than the essentially obsolete Pentium Pro) that has a dedicated, backside cache bus. All of today's Socket 7 processors must connect the L2 cache to the main system bus, which limits its clock speed and requires that the cache, main memory, and I/O traffic all share the same limited bandwidth. Increasing the Socket 7 bus to 100 MHz will boost this bandwidth by 50%, helping these processors continue increasing in performance as CPU clock rates rise. This short-term solution, however, still won't provide nearly as much cache bandwidth as even a half-speed backside bus.

In addition to adding a backside cache bus, the Pentium II design uses a different system bus than Pentium's—but a new bus is not necessary to implement a backside cache. In the second half of 1998, both AMD and IDT plan to introduce Socket 7 processors with 256K on-chip L2 caches. Thanks to 0.25-micron process technology, these chips will still be modest in die size (and thus in cost). Because the L2 cache interface remains on chip, it can run at the full processor speed without exotic interfaces or SRAMs. (A wider internal data path could boost bandwidth even more, but the companies plan to stick with a 64-bit path to minimize the changes to the CPU core.) At the same core CPU speed, an AMD K6+ or an IDT C6+ with a 256K on-chip cache could outperform a Pentium II with a 512K half-speed cache.

Putting aside the issue of the backside bus, Pentium II's other interface advantage is its P6 bus interface. With a highly pipelined design, this bus protocol allows multiple transactions to be overlapped more efficiently than in a Socket 7 system. As a result, it is far more effective in multi-

Intel Ships First Deschutes CPU

Intel today announced the first 0.25-micron Pentium II processor, code-named Deschutes. Running at 333 MHz, the new processor has the same features as the previous Klamath-based Pentium II but runs at a higher clock speed while consuming less power, thanks to a 2.0-V core supply; the L2 still runs at 3.3 V. Maximum power consumption is 23.7 W, 45% less than the 43 W consumed by the 0.35-micron 300-MHz part.

Power savings aside, the 11% clock-speed improvement isn't a very exciting change from the previous Pentium II processors. The interesting parts are yet to come: mobile versions, Slot 1 modules with a 100-MHz system bus, Slot 2 modules with large full-speed caches, and versions with clock speeds up to 450 MHz. Processors with all of these features, except for the highest clock speeds, should debut by midyear; the 450-MHz parts are due by year-end.

The Deschutes die is 131 mm^2, two-thirds the size of the 0.35-micron Klamath. Estimated manufacturing cost for the CPU die, according to the MDR Cost Model, is cut from about $85 for Klamath to about $65 for Deschutes; the module and cache RAMs add another $20 or so. The Deschutes module uses denser SRAMs for its L2 cache, implementing the 512K cache in two chips instead of four, as in the Klamath module.

The 333-MHz Pentium II is priced at $722 in 1,000s.

Pentium/MMX's Final Boost

Intel has announced a 266-MHz version of Pentium/MMX, using the 0.25-micron Tillamook design. The company is also offering a 166-MHz Tillamook; previous 166-MHz Pentium/MMX chips used the 0.35-micron design and thus consume more power. These processors are offered for mobile systems only, in either TCP packages or as part of a Mobile Module.

With a 1.8-V core supply, the 166-MHz part consumes 2.9 W typical; the 266-MHz chip requires a 2.0-V supply and dissipates 5.3 W typical.

When introduced on January 12, the 266-MHz processor was priced at $659, and the 166-MHz version was $300, both in 1,000s. On January 26, these prices were cut to $466 and $161, respectively. Mobile Module versions are $73 more.

processor systems. But since it has the same 64-bit width as the Socket 7 bus and runs at the same speed (66 MHz today, 100 MHz later this year), it has no fundamental bandwidth advantage in a single-processor system—and its latency is worse, though this is not an issue because memory systems are slower than the minimum bus latency in any case.

The technical advantages of the P6 bus (as distinct from the L2 cache architecture) in a uniprocessor system are that it can handle bus snooping more efficiently and can support out-of-order bus transactions. These capabilities may provide a small performance boost in some systems, but they are unlikely to make an overwhelming difference.

A processor with an on-chip L2 cache and a Socket 7 bus should be an excellent technical solution for single-processor systems, at least through 1998 and into 1999. Unless multiprocessor systems become mainstream, Socket 7 won't really break down, from a technical perspective, until it becomes necessary for the system bus to run faster than 100 MHz. The P6 bus, because it uses GTL+ signal levels and is highly pipelined, eventually will be able to run at much higher clock speeds than the Socket 7 bus. As main-memory bandwidth increases, a 100-MHz bus will become inadequate; assuming the bus width remains 64 bits, for example, a 200-MHz bus will be required to access the 1.6 Gbytes/s that will be delivered by a single bank of Direct RDRAMs.

The major hurdle facing sellers of Socket 7 systems is not technical but marketing. As Intel pushes Pentium II processors from the top to the bottom of the PC industry this year, it will make a massive investment in advertising and other promotions to convince users that anything less than Pentium II is inferior technology. Regardless of the technical issues, Intel is likely to succeed in moving most of the market to Slot 1, pushing even the best Socket 7 systems to relatively low price points by the end of 1998.

Moving Pentium II Into Entry-Level Systems

To move Pentium II (and Slot 1) all the way down to entry-level systems, Intel plans two new variations that will roll out during the second half of the year. The simplest, code-named Covington, is a Pentium II that lacks any L2 cache. This processor will be considerably slower than a standard Pentium II. With the L2 cache gone, there is very little technical advantage to the Slot 1 design, and Covington will be slower than Pentium/MMX processors at the same clock speed. Even a Pentium/MMX-233 may be faster than a Covington-266 on typical business applications. Nevertheless, cost-conscious consumers who have been trained to look for the Pentium II brand will find products they can afford.

Covington's value depends on its price. If Intel were to price a 266-MHz Covington lower than a Pentium/MMX-233, it could be a reasonable choice. So despite any technical merit, Intel can make this part succeed if it prices it aggressively enough. (Today, Slot 1 chip sets and motherboards carry a significant price premium, but most of this difference is likely to evaporate as Slot 1 volumes increase.)

Intel also plans to introduce a version of Pentium II, code-named Mendocino, with a 256K L2 cache integrated on the processor chip rather than in separate chips in the module. This processor follows the same strategy that AMD and IDT are following with Socket 7, but with a Slot 1 bus.

With the L2 cache integrated (or eliminated), the module packaging becomes vestigial; it is likely to remain for mechanical compatibility, though perhaps in a cost-reduced form, but there will be only one chip in the module. Sticking with the modular design will allow a PC maker to use one motherboard for a wide range of systems.

Intel is likely to offer Mendocino as a surface-mount chip as well as in a module, at least for notebook systems. For most systems, Intel is likely to stick with modules—even if they have only one chip—but for notebooks, the size and weight savings from eliminating the module can be significant, especially for the thinnest systems.

Slot 2 Moves Pentium II Upscale

While cacheless and integrated-cache versions of the Slot 1 module push Pentium II into entry-level systems, Slot 2 modules will address the needs of high-end workstations and servers. The Slot 2 module supports larger L2 caches running at the full processor speed, using custom Intel-built SRAM chips. Intel has not yet disclosed the exact size of the Slot 2 module or the specifications for the interface.

Intel's goal with Slot 2 modules is not to boost the performance of mainstream PCs, which would benefit relatively little from the large, fast caches, but to provide a high-end solution for multiprocessor workstations and servers. It is unlikely that Slot 2 modules will ever move down into mainstream PCs. The ability of Slot 2 modules to support four-processor systems, as well as dual-processor designs, is unlikely to make any difference in mainstream desktops. And as long as Slot 2 modules require Intel-made SRAMs, which

are needed to reach the performance goals, Intel is unlikely to bring the price down to the level required by mainstream systems; the opportunity cost to Intel of using its leading-edge fab capacity for SRAMs is just too high. Top-of-the-line Slot 2 modules will set new records for Intel microprocessor performance—and price.

Low-Cost PCs Play to Competitors' Strengths

The biggest shift in the PC market in 1997 was the emergence of sub-$1,000 PCs. According to Computer Intelligence, this price class rose from 7.2% of the U.S. retail market at the start of the year to more than 30% (in units) by the end. These systems are the leading edge of a phenomenon that is apparent, but less obvious, across the board: PC price points are dropping significantly. Computer Intelligence estimates that the average selling price of desktop PCs in the U.S. retail channel fell from $1,790 in January 1997 to $1,329 in November. The reductions are due to many factors, including lower DRAM and disk prices and increased manufacturing and distribution efficiencies as well as less-expensive microprocessors.

Regardless of the cause, this trend plays into the hands of Intel's competitors, whose main selling point has been low prices. As costs get squeezed, PC makers are more willing to accept a non-Intel processor because of the significant savings that are possible—and price-conscious PC buyers are often willing to compromise on the brand.

Indeed, it was the push for minimum cost that drove Compaq to adopt a Cyrix processor for its entry-level desktop system in early 1997. Cyrix's MediaGX, which powered the Presario 2100 and 2200, played a key role in launching the sub-$1K market. Although the MediaGX has lagged in features, such as USB and 3D acceleration, it provides a less expensive solution than any other processor: the processor and south-bridge chip (sold together) cost less than any other processor in the same performance class. Furthermore, no graphics chip, graphics memory, system-logic chip set, or sound card is needed.

Integration is not the only way to attack the sub-$1K market, however: all vendors, including Intel, have trimmed the prices of the lowest speed grades to serve the entry-level market. Compaq recently switched its $799 offering from the 180-MHz MediaGX to the 200-MHz K6, dropping integration and adding expansion slots and MMX while keeping the price constant (see sidebar, next page). Cyrix claims that Compaq's margin is much lower with the nonintegrated solution and hopes to regain the Compaq design win after it ramps up volume on the MediaGX/MMX.

Showing that even an Intel processor can be used in sub-$1K systems, HP's new $799 Pavilion 3260 uses a Pentium/MMX-200. Even at this entry-level price, HP chose to use the $106 200-MHz processor rather than Intel's current bottom-of-the-line 166-MHz version, priced at $95.

Intel has dropped the non-MMX Pentium from its lineup, resulting in an increase in its minimum price point (see MPR 1/26/98, p. 4). Intel's bottom-of-the-line price, which hovered at $106 for a year and a half, fell to $85 in the second half of 1997 but is now back up to $95—a curious change, given Intel's professed interest in the low-cost PC market.

Cyrix Ships MediaGX/MMX

Cyrix has added an MMX-enhanced version to the MediaGX product line, with the catchy name of MediaGX with MMX-Enhanced Technology. Initially offered only in a version aimed at mobile systems, the chip runs at 200 MHz, uses a 2.9-V core supply, dissipates 6 W maximum, and is priced at $114 in 1,000s. It debuted in Compaq's Presario 1220 notebook (see sidebar, next page).

The new chip differs functionally from the original MediaGX in two ways. First, the FPU was replaced with the FP/MMX unit from the 6x86MX, adding MMX capability and slightly boosting the FP performance. Second, the EDO DRAM controller was replaced with a 100-MHz SDRAM controller. Because of the change in the DRAM interface, the new chip is not pin-compatible with the older one and requires a revised board design.

The new processor uses the same IBM 0.35-micron CMOS-5X2 process, but the number of metal layers was increased from three to four. The additional routing density enabled the new features to be added with little increase in die size: the MediaGX/MMX, at 142 mm^2, is 6% larger than the non-MMX MediaGX.

Cyrix plans to shrink the chip to IBM's 0.3-micron CMOS-5X9 by the second quarter, boosting notebook clock speeds to 233 MHz and, in 3Q98, 266 MHz. This version measures 112 mm^2. Cyrix plans to move to a 0.25-micron process, probably in National's fab, leading to a 300-MHz part by the end of the year. Lower supply voltages should enable these clock speeds to be achieved with no increase in power consumption. Desktop versions will increase in clock speed more rapidly, since they are not constrained by power consumption.

A new version of the south-bridge chip, called the 5520, will debut soon and add USB capability and color-space conversion. Also due soon is the 9210 interface chip for passive LCD displays; this will be the first Cyrix chip to be built in a National fab.

AMD Dependent on 0.25-Micron Ramp

AMD successfully launched the K6—the first tangible result of its NexGen acquisition—in the spring of 1997. AMD has been selling everything it can produce but has not been able to ramp up volume in Fab 25 as quickly as it had hoped. After shipping 350,000 units in 2Q97, AMD aimed for 1.5 million in 3Q97 but shipped only 1 million. It then aimed for 2 million in 4Q97 but shipped only 1.5 million, for a total of just under 3 million K6 units in 1997. AMD also shipped about 2.5 million K5 processors, plus 1.6 million 5x86-133 chips

Compaq Uses Cyrix, AMD Chips

In a sweeping revision of its Presario line announced January 6, Compaq—the world's largest PC maker—has given Intel's competitors their strongest endorsement yet. For the first time, Compaq is using non-Intel processors in a notebook computer and in all of its low-cost consumer desktops. Intel-based systems remain in the Presario line but are limited to higher price points. The business-oriented Deskpro line remains entirely Intel-based.

The new Presario 1220 notebook, priced at $1,999, uses Cyrix's MMX-enhanced MediaGX processor, running at 200 MHz. The MediaGX, although it has an integrated display controller, cannot drive a passive-matrix LCD without an additional interface chip. Compaq decided to use a NeoMagic LCD controller instead, leaving the display controller in the MediaGX unused.

The next step up, the Presario 1621 notebook, marks AMD's first notebook design win. Based on a 233-MHz K6 (built in 0.25-micron technology), the system is priced at $2,499. Compaq also offers a "small business" notebook, based on an Intel Pentium/MMX-166 for $2,299; an Intel-based multimedia notebook, with a TFT display and a 233-MHz Pentium/MMX, is $2,999.

The MediaGX has been booted out of the desktop product line, however; Cyrix was unable to meet Compaq's volume needs for both desktop and notebook systems at the start of the MediaGX/MMX production ramp. The MediaGX-based Presario 2200 has been replaced with the 2240, using a 200-MHz AMD K6 processor. This system retains the $799 price of the former model.

The next step up is also K6-based: the Presario 4540 system, priced at $1,099, uses a 233-MHz K6. A more robust configuration is available as the 4550 for $1,299.

There are no Pentium/MMX-based systems in the Presario desktop line. Pentium II systems run $1,799 for 266 MHz or $1,999 for 300 MHz. These systems include DVD drives and AGP graphics.

By using AMD and Cyrix processors for all of its least-expensive consumer notebook and desktop systems, Compaq has ensured that a significant part of its volume will shift from Intel to AMD and Cyrix.

(also known as the 486DX5) into the PC market. AMD's total PC processor shipments for the year were just under 7 million units, or about 8% of the market.

A combination of factors, presumably related to fab changes made to accommodate the K6's IBM-like process, contributed to poor yields, especially at the highest speed grades. Making matters worse, Intel slashed its Pentium prices midyear, forcing AMD to respond with deep price cuts. This combination of factors made for an unhappy financial picture.

AMD hopes to ship about 15 million units in 1998—2.5 times its run rate in 4Q97 and about 15% of the total market. The increase in capacity will come primarily from conversion of the K6 to 0.25-micron technology. With a die size of only 68 mm^2, the 0.25-micron K6 should produce more than three times as many working chips from each wafer as the 162-mm^2 0.35-micron version.

AMD is currently shipping 0.25-micron processors from its Submicron Development Center in Santa Clara and is beginning production using this process at Fab 25 in Austin. The 0.25-micron parts have not been formally announced, even though IBM has announced a K6-266 desktop system and Compaq has announced a K6-233 notebook, both using the 0.25-micron chips. Apparently, these two customers will consume all the near-term production. Curiously, IBM is calling the chip the IBM K6; IBM negotiated the right to use this name as part of an agreement to provide C4 solder-bump processing under contract to AMD.

The K6 3D and K6+ 3D will be larger than the 0.25-micron K6 but still much smaller than the original K6. The 3D extensions and on-chip cache should boost prices. The trick, as always, will be to get these chips into volume production at each performance level before Intel relegates that speed grade to the economy bin.

AMD's design wins at Compaq and IBM show confidence is building that the company can deliver the K6 in volume. If AMD can achieve a smooth transition to 0.25-micron production and to the new K6 versions, it could do quite well in 1998. Further hiccups, on the other hand, could undermine not only AMD's near-term financial performance but also longer-term PC maker confidence. AMD should have an exceptional opportunity as the first to ship a processor with 3D extensions—the biggest feature advantage AMD has ever had over Intel—just in time for a new release of Microsoft's DirectX software that will support it.

Cyrix Extending Integration Push With GXm, MXi

Cyrix attacked the market in 1997 with a two-pronged thrust: MediaGX for the entry level and 6x86MX for the mainstream. Both product lines will get updates in '98, with the integrated line leading the way.

Cyrix has remedied the MediaGX's lagging feature set with the MediaGX with MMX (see sidebar, previous page). Coupled with a second-generation south bridge chip due to be announced shortly, it will keep the MediaGX solution from falling off the bottom of the performance spectrum. But because Intel is moving Pentium/MMX down to the low end—at 166–200 MHz this quarter and 200–233 MHz next quarter—these changes really just keep pace.

Cyrix plans to make a dramatic move up the performance curve in its integrated line with a part code-named the MXi (and not yet officially named). The MXi will be the first chip to incorporate the Cayenne core, a third-generation enhancement of the 6x86 design. Cayenne will provide a fully pipelined floating-point unit and a dual-issue MMX unit,

matching the capabilities of Intel's chips, and it will include 3D instruction-set extensions compatible with the AMD/Cyrix/IDT standard. Cyrix expects the Cayenne core to run at speeds of 250–350 MHz while delivering performance up to that of a 400-MHz Pentium II. The MXi's performance will be boosted further by a capable 3D rendering engine and a 133-MHz SDRAM interface, giving it the potential to be a great processor for low-cost, entertainment-oriented PCs.

Other Plans Beyond 6x86MX Unclear

Cyrix plans to increase 6x86MX performance steadily during 1998 through a series of process shrinks, nearly one per quarter. The company is targeting top performance levels of PR266 this quarter, PR300 in the second quarter, and PR350 in the third quarter. The third-quarter version is based on 0.25-micron technology and will be the first Cyrix processor to use C4 bonding, as well as the first to be built by National as well as by IBM.

The die size for this version will be 68 mm^2 in IBM's CMOS-6X process, matching that of AMD's K6. Cyrix has already produced samples of 0.25-micron 6x86MX processors at National's development line in Santa Clara, with a die size of 88 mm^2. It expects to begin producing the 0.25-micron chip using National's South Portland, Maine, fab by midyear.

Cyrix has declined to describe any chips that will be based on the Cayenne core, other than the highly integrated MXi. Company officials have cagily agreed that more bandwidth than Socket 7 can provide is needed to sustain this core, but they have not been willing to explain their solution.

Cyrix's options are to stick with Socket 7 but integrate the L2 cache, as AMD is doing with the K6+; skip to a higher-performance but incompatible bus, as AMD has disclosed it will do with the K7's "Slot A"; or build a Slot 1–compatible module. The last of these alternatives may be the most attractive. Cyrix has been openly critical of AMD's Slot A approach, and an extended Socket 7 strategy doesn't have enough long-term potential.

AMD traded away its right to build Slot 1 processors in return for its Intel patent license in 1995, but IBM and National made no such deal; their licenses are unrestricted. One concern is the potential for system-level patents that Intel could assert against PC makers using a non-Intel Slot 1 processor. If National is willing to take this risk, however, being the only alternative supplier of Slot 1 processors could be an attractive position.

Cyrix Living With Lower Prices

Although Cyrix, along with its partner IBM, shipped about as many processors in 1997 as did AMD, many of these chips were low-priced MediaGX chips that pushed down the average price. While AMD achieved an average selling price of around $150 in the third quarter and $125 in the fourth quarter, for example, Cyrix's ASP was near $70. Cyrix and IBM together shipped a total of about 6.5 million processors, including 3 million 6x86s, 1.4 million MediaGXs, and

Key x86 Events of 1997

Intel started the year with Pentium/MMX (1/27/97, p. 4) at up to 200 MHz and later boosted it to 233 MHz (6/2/97, p. 4). Pentium/MMX was the first to move to 0.25-micron CMOS (5/12/97, p. 4) (9/15/97, p. 4).

Pentium II (2/17/97, p. 1) (5/12/97, p. 1) debuted at 233–300 MHz. Intel laid out the strategy for Slot 1 and Slot 2 (8/25/97, p. 10), acknowledged a secret Pentium II feature that allows Intel to deliver microcode patches via the BIOS (9/15/97, p. 16), and disclosed plans for low-cost Pentium II variants (11/17/97, p. 4).

A bug was found in Pentium/MMX that enables a malicious user to crash certain systems (11/17/97, p. 4), but OS workarounds are possible (12/8/97, p. 5).

In addition to its regular quarterly price cuts (2/17/97, p. 27) (5/12/97, p. 23) (8/4/97, p. 27) (10/27/97, p. 39), Intel slashed Pentium/MMX prices midyear to drive the transition to MMX (7/14/97, p. 1) (8/4/97, p. 4).

Intel introduced a 1M cache version of Pentium Pro, setting a new high in x86 price points (8/25/97, p. 5).

Intel sought to acquire C&T (8/25/97, p. 4) and succeeded in acquiring Corollary (10/27/97, p. 5).

Intel sued AMD and Cyrix over their use of MMX as a generic term (3/31/97, p. 4), and the competitors later agreed to credit Intel with the trademark (5/12/97, p. 9).

Intel was sued by both Cyrix and Digital for patent infringement (6/2/97, p. 26), and by Intergraph for patent infringement and other anticompetitive behavior (12/8/97, p. 4).

AMD launched the K6 (3/31/97, p. 1) and then at the Forum described the future K6 3D and K6+ 3D (10/27/97, p. 19). Cyrix and IDT agreed to make their 3D extensions compatible with AMD's (12/8/97, p. 4).

Cyrix introduced the MediaGX at 120 and 133 MHz (3/10/97, p. 1) and later moved to 166 and 180 MHz (7/14/97, p. 4). Cyrix described at the Forum its next integrated processor, the MXi (12/8/97, p. 16).

Cyrix replaced the 6x86 with the 6x86MX (6/2/97, p. 12). IBM laid out a roadmap for speed boosts (10/6/97, p. 4), and Cyrix described the next-generation Cayenne core at Microprocessor Forum (10/27/97, p. 22).

Cyrix closed the year by being acquired by National (8/25/97, p. 1) (12/8/97, p. 5).

National described the N7, a P5-class integrated NC chip, at the Forum (10/27/97, p. 16).

IDT, using designs from its Centaur Technology subsidiary, joined the x86 battle with the C6 (6/2/97, p. 1). At Microprocessor Forum, Centaur described the future C6+ and C6+ w/L2 versions (11/17/97, p. 17).

Benchmark results showed the FP and MMX performance of AMD's and Cyrix's chips lagged that of Intel's chips (9/15/97, p. 18).

2 million 6x86MXs, giving them a combined market share of about 7%.

The public plans of the two companies imply AMD will lead Cyrix in moving up the speed curve, and it will also be in the market with 3D instruction-set extensions several months earlier. Assuming the company can achieve its production ramp-up, this should keep AMD on a course to generate significantly more revenue than Cyrix in 1998.

One wild card is Cyrix's MXi. This could be a hot product, but there are too many unknowns: when it will ship, what performance level it will deliver, and how much Cyrix will be able to charge for it. Cyrix's plans for a more conventional implementation of the Cayenne core remain a mystery, and its future in late 1998 and into 1999 will depend on this unknown.

Another unknown for Cyrix is how National's proclaimed strategy of focusing on highly integrated, low-cost designs for smaller-than-PC devices will affect Cyrix's future product line. The vision of hundreds of millions of information appliances per year, each with a single-chip PC subsystem inside, is a grand one, and it may someday come to pass—but it isn't going to happen soon, and the profit on each of those single-chip PCs will be small.

National must continue to focus on the existing PC market if it is going to get its value out of Cyrix. One effect of the merger is already apparent: development of National's own 586L CPU core has been canceled, and future products for the embedded and network-computer markets will be based on Cyrix cores.

Cyrix projects its x86 capacity in 1998 to be more than 10 million units but acknowledges that it may not be able to sell that many chips. This capacity comes from a combination of three manufacturing resources: IBM, National's South Portland fab, and Asian foundries. Now that Cyrix is part of National, which has an Intel patent license, it is free to use any foundry.

IDT Just Getting Started

Centaur Technology has taken over Cyrix's original role as the tiny player among the x86 suppliers, focused on the low end of the market. Unlike Cyrix, however, Centaur has been part of a fab-based semiconductor company from its founding. And unlike AMD, IDT is not trying to fill an entire large fab with x86 processors: it is seeking (and has capacity for) only a small share of the market, so it is focusing on smaller PC makers. Its first major customer is not a PC maker at all, but Evergreen Technologies, which sells the chip as an end-user upgrade for existing PCs.

IDT began shipping the C6, the first processor in its WinChip family, in October, at clock speeds of 180 and 200 MHz. A 225-MHz version shipped late last year, and a 240-MHz part is due this quarter. The C6 has the lowest power consumption of all the Pentium competitors except the MediaGX, even without using a split rail (the core runs at 3.3 V along with the I/O).

Around midyear, IDT plans to replace the C6 with the C6+, incorporating a much faster FPU, dual-issue MMX unit, 3D instruction-set extensions, and numerous small enhancements to boost performance. These enhancements should enable the WinChip family to gain ground on the low end of Intel's product line. IDT plans to introduce the C6+ simultaneously in both 0.35- and 0.25-micron technology; the 0.25-micron die size is a mere 58 mm^2, the smallest in the industry. IDT claims the C6+ will have 10% better Winstone performance than the C6 at the same clock speed, plus twice the throughput on FP and MMX operations.

Like AMD, IDT plans to introduce in the second half of the year a processor with an on-chip 256K L2 cache. For IDT, which has earned much of its living selling SRAMs, this is a natural evolution—in fact, one might think of this product as an SRAM with an integrated processor, dramatically increasing the SRAM's value.

IDT has no patent cross-license with Intel, but no legal action has been taken. Intel may have decided to leave IDT alone to avoid provoking the FTC any further. IDT also has patents, especially on SRAMs, that Intel may find itself accused of infringing should it bring suit against IDT.

No Easy Victories

Intel's competitors have found the going rough for the past few years, and 1998 doesn't look like it will be much easier. All three competitors have a good shot at gaining market share, and Intel's share is almost sure to shrink during the year—but it will be surprising if Intel's share of the x86 PC microprocessor market drops below 75%. As long as the PC market itself sees robust unit growth, Intel should do well. One of Intel's challenges will be to increase its average selling price through a migration to Slot 1 and Slot 2 processors, even as the ASP of PCs may continue to decline.

For AMD, Cyrix, and IDT, the question of how long the midrange of the market will remain interested in Socket 7 processors, no matter how fast they are, will be a critical one as 1998 progresses. Intel will seek to make the transition happen quickly—both to increase its ASPs and to make it harder for its competitors to sell their products.

The biggest challenge for Intel's competitors will be to increase clock rates faster than Intel can slash the prices associated with the performance points the competitors deliver. With Intel moving aggressively to 0.25-micron technology, its competitors must quickly follow suit to keep pace.

Intel's competitors will have two key technologies in 1998 that Intel will not: Socket 7 processors with an integrated L2 cache and processors with 3D instruction-set extensions. Transition years have traditionally been good opportunities for Intel's competitors to gain market share by offering more advanced chips using the interface Intel is leaving behind. Within the Socket 7 pinout, Intel's competitors will have much faster processors than Intel, putting them in a stronger position than in recent years—as long they can resist the Slot 1 tide. M