by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,640,533

Translation lookaside buffer (TLB) arrangement wherein the TLB contents are retained from task when it is swapped out and reloaded when the task is rescheduled
Issued: June 17, 1997
Inventors: Kirk Hays, et al
Assignee: Intel
Filed: December 13, 1995
Claims: 9
A method and apparatus for using a TLB for maintaining page tables in a paging unit on a computer system. The TLB contents for executing tasks are saved when the task is swapped out. The contents are then reloaded into the TLB when the task is again scheduled for execution.

5,640,588

CPU architecture performing dynamic instruction scheduling at time of execution within single clock cycle
Issued: June 17, 1997
Inventors: Anantakotiraju Vegesna, et al
Assignee: Ross Technology
Filed: January 29, 1996
Claims: 8
Apparatus and methods for scheduling a sequence of instructions for achieving multiple launches and multiple executions of the instructions within a central processing unit. Each of the instructions is classified according to which one of multiple processor execution resources executes the instruction. The classifications associated with the instructions occur in the order in which the instructions occur in the sequence.

5,640,503

Method and apparatus for verifying a target instruction before execution of the target instruction using a test operation instruction which identifies the target instruction
Issued: June 17, 1997
Inventors: Alan Ian Alpert, et al
Assignee: IBM
Filed: June 7, 1995
Claims: 19
A Test Operation-Code (TSTOP) instruction preverifies the validity of a target instruction opcode prior to execution. The preverification function sets a return value in a program status word to indicate whether the opcode is valid, present on the CPU, not present on the CPU, or other conditions.

5,640,526

Superscalar instruction pipeline having boundary identification logic for variable length instructions
Issued: June 17, 1997
Inventors: Stephen William Mahin, et al
Assignee: IBM
Filed: December 21, 1994
Claims: 16
A mechanism to manage variable length instructions in a cache is comprised of three cooperating elements which optimize self modifying code and anticipate next instructions for branch operand management.

5,638,525

Processor capable of executing programs that contain RISC and CISC instructions
Issued: June 10, 1997
Inventors: Gary N. Hammond, et al
Assignee: Intel
Filed: February 10, 1995
Claims: 19
Apparently, the first U.S. Merced patent. A processor and methods for executing multiple instruction sets on a single CPU. The apparatus and methods include multiple strategies for translating CISC instructions to RISC, or executing CISC instructions natively, including multiple register sets.

5,636,352

Method and apparatus for utilizing condensed instructions
Issued: June 3, 1997
Inventors: Richard Bealkowski, et al
Assignee: IBM
Filed: December 16, 1994
Claims: 15
A processor that fetches compressed "synonym" instructions, internally converts the synonym instructions to actual instructions from a storage bank, and executes actual instructions.

5,636,351

Performance of an operation on whole-word operands and on operations in parallel on sub-word operands in a single processor
Issued: June 3, 1997
Inventor: Ruby B. Lee
Assignee: HP
Filed: February 17, 1995
Claims: 32
A system allows parallel processing in a single processor by partitioning an ALU or shifter. In a full-word mode, data is allowed to propagate across the partitions. In partitioned mode, data is not propagated across the partitions. M