Lexra ASIC Core Dupes MIPS R3000

LXR-4080 Is Independent Implementation of Basic MIPS-I Processor Core

by Jim Turley

A small Massachusetts startup is paying MIPS the sincerest form of flattery—without paying royalties. Lexra Computing Engines is offering its own interpretation of the MIPS R3000 microprocessor core for ASIC development. Like MIPS licensees Toshiba, NEC, LSI Logic, and others, Lexra is banking on the growing popularity of embedded microprocessor cores. Unlike those other companies, however, Lexra has not obtained a MIPS license.

The company was undaunted by the technical challenge of developing a MIPS-compatible microprocessor and seems equally undaunted by the legal challenge. The firm believes it has infringed no patents or other intellectual property. Lexra indemnifies its customers from legal attack as part of its standard licensing agreement. And its prices undercut those of the approved core licensees, starting at just a few hundred thousand dollars plus royalties.

Hurdles More Legal Than Technical

There are certainly many precedents in the microprocessor industry for copying or cloning instruction sets. AMD and Cyrix, for example, turn out 486- and Pentium-compatible processors by the millions without infringing copyrights, patents, or other intellectual-property rights. We expect more x86-compatible cores to appear soon. DSP cores compatible with TI's popular 'C50 and 'C30 product lines are available, also without legal challenge. And Motorola just licensed its own 68K core from a Japanese company that reverse-engineered it (see MPR 12/29/97, p. 11).

With MIPS trailing only the 68K and x86 in popularity (see MPR 1/26/98, p. 14), it has fallen prey to similar treatment. MIPS and ARM both require semiconductor vendors to acquire a license, usually to the tune of several million dollars. In return, vendors are free to produce instruction-set–compatible processors. ARM prohibits its licensees from altering or extending the instruction set in any way; MIPS allows a bit more freedom. MIPS licensees can develop one-of-a-kind products with special features for unique applications. These microprocessor "mules" cannot reproduce, however, and are limited to a single generation.

Instruction sets, per se, cannot generally be patented or copyrighted. (Mnemonics can, but vendors get around this by not printing programmers' reference manuals.) Internal microarchitecture, on the other hand, is often protected under patent law by citing specific circuit-design techniques. Thus, if a different microarchitecture (circuit design) can be developed that executes the same instruction set and produces the same results, it is generally legal to produce.

Silicon Graphics disputes Lexra's claim that it infringes no MIPS-related patents. SGI believes that certain aspects of the MIPS instruction set are, in fact, covered by patents, but it was unable to cite any. In the company's view, there can be no way to execute MIPS binary instructions and produce MIPS-compatible results without infringing SGI's rights. SGI is currently "looking into" Lexra's legal status.

Part Emulates R3000 Processor, Mostly

On the surface, the 4080 behaves like any of a number of early MIPS cores, such as LSI Logic's CW4001 (see MPR 12/26/94, p. 15), Toshiba's TX19 (see MPR 2/16/95, p. 20), or NEC's R4010 (see MPR 3/27/95, p. 12). The core runs at about 100 MHz in 0.35-micron technology and executes most—but not all—of the MIPS-I instruction set. The exceptions are multiply, divide, and unaligned loads and stores. In addition to their being difficult to implement, we suspect Lexra may have found these features had better legal protection than the rest of the CPU, but the company would not confirm this.

Under the surface, the 4080 has a conventional five-stage pipeline, a three-port register file, and a Harvard bus structure. There is a separate adder for branch-target calculations. Lexra has achieved 102 Dhrystone MIPS in simulation, a bit lower than the 1.2–1.3 MIPS/MHz ratio that's now typical of 32-bit RISC processors.

Lexra distributes the 4080 as either a synthesizable model or a physically arranged "hard macro" targeted for specific fabrication processes. Either way, the package comes with more than just an execution engine.

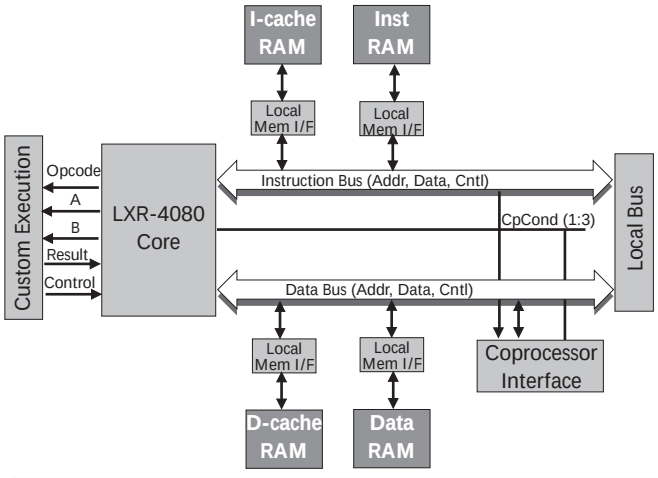

Figure 1. Lexra's LXR-4080 MIPS core includes, at a minimum, the CPU, two caches, and an internal bus interface. The CPU core can be extended either with coprocessors or with custom logic.

The minimum standard configuration consists of the LXR-4080 processor core (with three-port register file and CP0 coprocessor), a 32-bit instruction bus (with address, instruction, and control signals), a 32-bit operand bus (also with address, data, and control signals), an instruction cache, a data cache, and an on-chip bus interface. Figure 1 shows the arrangement of these basic structures. In addition to the mandatory instruction and data caches, the user can add instruction and/or data RAM or ROM as desired.

The CPU is expandable in two ways: either through coprocessors or by adding execution units. Coprocessors are MIPS-standard extensions to the basic CPU that are accessed via instructions addressed to specific coprocessors (CP1, CP2, etc.). Many MIPS chips implement the FPU this way.

The customer-specific extensions are unique to Lexra's implementation. Lexra allows its licensees to add execution units and/or instructions to the base CPU by tapping directly into the CPU core. Lexra's synthesizable model breaks out all the signals—including a 12-bit opcode-field, two 32-bit operand buses, a 32-bit result bus, and synchronization signals—needed to attach extra execution units. Any unused MIPS opcodes may be used to enable the extra instructions.

The total LXR-4080 package consumes 8.5 mm^2 of 0.35-micron silicon, of which just 1.8 mm^2 is the 86,000-transistor CPU core itself, according to Lexra. Power dissipation, which can be somewhat speculative in the context of an ASIC core, is said to be 150 mW at 100 MHz and 3.3 V. In physical terms, the 4080 is quite competitive with similar cores from ARM, MIPS, SPARC, ARC, or ColdFire.

Branches Assumed Taken Rather Than Not

Lexra chose to deviate slightly from the way other MIPS chips handle branches. The 4080 has no branch prediction—which typically means all branches fall through by default—but operates as if all branches will be taken. All branches (conditional or not) flush the 4080's execution pipe and redirect the fetch stream to the target address. If the branch was, in fact, taken, there is no penalty. If, however, the branch should not have been taken, the 4080 pays a one-cycle penalty.

Reversing the conventional wisdom regarding branches improves typical performance slightly while adding nothing to the core's complexity. Most backward branches (loops) are taken, while forward branches are taken about half the time, so it is generally better to assume that all branches are taken rather than not.

Prices Much Lower Than Competitors'

Lexra's big competitive advantages over the licensed core vendors, it believes, are its pricing and its customers' ability to use almost any foundry. The company charges $210,000 for an RTL license to the LXR-4080, far lower than the millions of dollars charged by ARM or MIPS—which generally provide hard macros only, not portable models.

An unlimited license costs $550,000, about 2.6 times the one-time fee, and confers the right to use the 4080 in multiple products. An optional maintenance contract runs an extra 6% of the purchase price, or $12,600 per annum to start. Lexra also charges a per-piece royalty when a chip enters production. Maintenance fees can be applied toward royalties. Like the other core vendors, Lexra also offers its CPU as a hard macro, already placed and routed for approved semiconductor processes.

Unlike the big CPU vendors, Lexra deals directly with its end users (in this case, ASIC developers) rather than with semiconductor vendors. ARM and MIPS, in contrast, license semiconductor companies, which then lure customers. Lexra licenses its core to ASIC customers, which are then free to select whatever foundry or vendor they please.

Price & Availability

Lexra's LXR-4080 is available now as a Verilog model and as a prearranged hard macro. For more information, contact Lexra (Waltham, Mass.) at 781.899.5769 or visit *www.lexra.com*.

New CPU and DSP Cores Due in 1999

After the LXR-4080, Lexra is planning the LXR-4081, a newer MIPS core that adds MIPS-16 code compression, multiprocessing (with cache coherence), DSP enhancements (with multiply-accumulation), support for embedded DRAM, and "enhanced" real-time functions through lower-latency interrupts. Scheduled for the end of 1998, the 4081 is targeted for a 0.25-micron process and a 200-MHz clock rate. A planned MMU should allow it to run Windows CE.

Lexra's charter includes both RISC processors and DSPs. The proposed LXD-5080 is a 16-bit fixed-point DSP scheduled for production in 1999.

Lexra Off to a Modest Start

There's no question that Lexra is entering a growing, profitable market. Or that it should find willing customers eager to save on license fees and benefit from a broader choice of foundries. What is in question is the ten-person firm's recipe for staying out of legal hot water.

As Intel, Digital, AMD, and countless other firms have discovered to their detriment, the threatening clouds of legal entanglement can cast a dark shadow over a product, regardless of the merits of the case. For a company as young and small as Lexra, a delay of even a few months could be critical.

Lexra has four customers so far, which it declines to identify, so there is some evidence that companies are betting their products on Lexra's technology and business plan. If Lexra succeeds in promoting the LXR-4080 and in producing its follow-on products next year, it could drive a wedge into the intellectual-property market and embolden other IP vendors. If the company succumbs, those other vendors may need to rethink their strategies. M