National Kills In-House Embedded x86 Work

National Semiconductor has quietly pulled the plug on its in-house embedded x86 processors. The recently announced NS586L (see MPR 10/27/97, p. 16), which was to enter production this year, fell under the axe, and development of the N7 has also been canceled. The existing NS486SXL and 'SXF chips are unaffected. National's future x86 chips will be based on cores developed at Cyrix, which National bought last summer for $528 million (see MPR 8/25/97, p. 1).

The move resets several years of in-house development of x86-compatible chips at National. The company's NS486 (see MPR 9/11/95, p. 1) offered complete x86, but not PC, compatibility. By omitting features like the FPU, MMU, and real-mode operation, National was able to offer cut-rate parts to embedded designers. The integrated NS586L and proposed N7 parts were to follow the same theme, stripping the CPU core to the bone and adding peripheral I/O.

National's late-term cancellation of the NS586L suggests that customers weren't entirely happy with the lack of PC compatibility in their embedded chips. Although National would not confirm, we expect future Cyrix-based embedded parts will offer full PC compatibility, even if it costs a little extra in manufacturing. These new embedded parts probably won't reach production until 1999.

National said it expects to continue on in the spirit of the NS586L and N7, making low-cost, integrated processors for the PC and information-appliance markets, just not with the NS586 core. Overall, National's strategy of making application-specific PC processors won't change, only its choice of processor design teams. —*J.T.*

Motorola Core+ Chip Merges CPU With FPGA

Upping the ante for integration, Motorola has revealed plans for microprocessors with field-programmable gate arrays (FPGA) integrated onto the part. The first chip in the new Core+ family isn't expected until 3Q98, and pricing has not been set, but the new chip could mark the first time a 32-bit processor has been merged with user-programmable logic.

The first chip, christened MPACF250, will be based on a ColdFire v2 core, similar to that of the CF5206 (see MPR 9/11/95, p. 12). Also like the 5206, the '250 will include a 512-byte cache, 512 bytes of SRAM, a two-channel DMA controller, two UARTs, an I^2C interface, programmable I/O pins, and Motorola's background debug module.

The most interesting aspect of the '250, however, will be its on-chip programmable logic. The company has not yet divulged how many gates of equivalent logic the chip will include, how fast it will be, or any other technical specifications of the logic itself, other than to say it will cover about 90% of the total chip area. The programmable logic will be the first implementation of Motorola's 2000-series FPGA architecture, an upgrade from the fine-grained 1000-series FPGA chips Motorola has been selling for about a year. (More information is available at *mot-sps.com/fpga*.)

The technology in such a part may be interesting, but its application is unclear. The '250 does not add to the state of the art for either processors or FPGAs. Its major benefit is in space savings, by integrating the two devices into one. Customers who are currently using ColdFire CPUs and Motorola FPGAs may regain some board space, but it's not clear new customers will be lured by the combination.

Although makers of 8-bit and 16-bit microcontrollers have previously integrated modest amounts of programmable logic onto their parts, the Core+ family will be the first time for a 32-bit processor. Pricing will play an important role in the eventual success or failure of the Core+ family; if the chips are priced more than about 50% over the cost of the CPU and FPGA separately, customers may not see the benefit. Done right, though, this could be a popular combination for moderate-volume systems. —*J.T.*

QED Gets Airborne

Quantum Effect Design (*www.qedinc.com*) has signed an exclusive agreement with Aeroflex Circuit Technology (*www.aeroflex.com*) to provide high-end MIPS processors for use in harsh airborne or industrial environments. Aeroflex will supply both normally packaged parts and multichip modules that include QED's microprocessors. QED's entire product line of CPUs is included in the deal, but neither company would discuss pricing or availability.

The arrangement marks the first of its kind for MIPS chips. Currently, only a few 32-bit CPUs (e.g., 68K and i960) are available in industrial or military temperature grades. Most semiconductor vendors have found it too awkward or expensive to maintain high-grade parts for low-volume industrial applications. By shifting this burden to Aeroflex, QED gains a toehold in a new embedded niche. —*J.T.*

Motorola Joins Java Bandwagon

Motorola has signed a broad licensing agreement for Sun's Java technology, but both sides were vague about product plans. The pact calls for Motorola to license PersonalJava, EmbeddedJava, JavaCard, and the Java Application Environment (i.e., the run-time platform for desktop computers) to be deployed on unspecified systems in an unspecified time frame. The deal does not include Sun Microelectronics' PicoJava or MicroJava microprocessor hardware designs.

The deal was made at the top level of Motorola's byzantine hierarchy and involves more than just Motorola's chip-making operations. It appears Motorola will use Java software in future cellular telephones, smart cards, two-way radios, and computers. Combined with Motorola's new M•Core architecture, Java also appears destined for automotive systems. —*J.T.*