BUSES

Digital-camera interfaces lead to ubiquitous deployment. Low-cost digital cameras and evolving interfaces simplify video-capture tasks, while software developers tackle advanced edge- and motion-based algorithms for compelling visual applications. Maury Wright, *EDN*, 1/15/98, p. 63, 7 pp.

Designing a USB hub: basic options and issues. All peripherals connect to the Universal Serial Bus through hubs. How you design a USB hub depends on the purpose you want it to serve. Harry Inia, National Semiconductor, and Doug Dument, Computer Access Technology Corp.; *EDN*, 1/15/98, p. 113, 5 pp.

IC DESIGN

Designers tackle the testability of a system-level IC. To test and debut a 400,000-gate system on silicon with embedded processor, memory, PCI interface, and peripheral control logic, three different test strategies were needed. Ki Joo Jeong, LG Semicon, et al; *Integrated System Design*, 2/98, p. 38, 5 pp.

Power pushed to prominence by system-on-a-chip and portable products. Whether you develop your own methodology or use commercial tools to design your system ASIC for battery-powered applications, make low power your priority from specification to implementation, and keep your eye on emerging library standards. Barbara Tuck, *Computer Design*, 1/98, p. 49, 10 pp.

Focus report: High-speed ASIC benchmark. The effect of interconnect delays on deep-submicron designs forces designers to look beyond speed as the primary indication of circuit performance. R. T. Maniwa, *Integrated System Design*, 2/98, p. 48, 7 pp.

Redefining EDA in the new age of intellectual property. The emergence of core-based designs prompts the evolution of new EDA tools and the design issues that need to be addressed. Cheryl Ajluni, *Electronic Design*, 1/12/98, p. 64, 8 pp.

Defining where IP fits in future communications design. Despite its growing pains, intellectual property will play a key part in developing the system chips to power tomorrow's communications products. Tony Parker, *Electronic Design*, 1/12/98, p. 93, 4 pp.

IP fuels a transformation of culture, companies, and cooperation. System and chip design will take place concurrently, and today's silicon designers will become tomorrow's system integrators. Steve Glaser, *Electronic Design*, 1/12/98, p. 55, 4 pp.

Optimizing at the system level means incorporating IP from many sources. Combining fixed intellectual property (IP) to achieve a system-design specification will be a stop-gap method until system-level synthesis arrives. Charles H. Small, *Computer Design*, 1/98, p. 68, 4 pp.

MEMORY

EEPROM: Survival of the fittest. EEPROMs are expanding and transforming their features to meet evolving application needs and competitive pressure. Brian Dipert, *EDN*, 1/15/98, p. 77, 9 pp.

MISCELLANEOUS

Kaffe anyone? Implementing a Java virtual machine. If the popularity of Java-related presentations at the most recent Embedded Systems Conference in any indication, quite a few embedded programmers are considering adopting this much-publicized new language. Michael Barr, TSI TelSys, and Jason Steinhorn, Hughes Network Systems; *Embedded System Programming*, 2/98, p. 34, 9 pp.

The VSI alliance: the journey from vision to production. The alliance is making system-on-a-chip design a practical reality through the mixing and matching of virtual components. Douglas Fairbairn and Diana Anderson, Cadence; *Electronic Design*, 1/12/98, p. 86, 4 pp.

Windows CE—new software force in embedded? The release of Windows CE 2.0 moves that operating system into more mainstream embedded devices, but will this be the unifying software force of the embedded world? Rick Grehan, *Computer Design*, 1/98, p. 81, 5 pp.

Information appliance: gadget netoptia. While successful Information appliances do multimedia, e-mail, fax, and other functions inherited from their PC parents, they must do it much better than the current machines. Ted Lewis, *Computer*, 1/98, p. 59, 10 pp.

Speech and text entry systems speak softly and carry small styli. In an age of shrinking displays and keypads, speech and handwriting recognition is providing an intuitive interface. Cheryll McKinnon, *Portable Design*, 12/97, p. 20, 7 pp.

SYSTEM DESIGN

Designing fast Ethernet switches is easy with chip sets and reference kits. Designing Ethernet switches has never been easier; off-the-shelf switch chips and reference designs dramatically reduce switch development costs. Stephen Kempainen, *EDN*, 1/1/98, p. 59, 7 pp.

Notebook computer makers address power challenges. Manufacturers are uniting behind the Mobile Power Initiative, a coordinated industry program. Rex C. Peairs, Intel; *Electronic Design*, 12/15/97, p. 44, 3 pp.

Evaluating ASIC memory trade-offs. On-chip memory and a small cache can increase performance when you're using an embedded RISC core. Mark Buchanan, *Integrated System Design*, 2/98, p. 15, 5 pp.