by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,649,138

Time-dependent rerouting of instructions in plurality of reservation stations of a superscalar microprocessor
Issued: July 15, 1997
Inventor: Mark A. Ireton
Assignee: AMD
Filed: January 4, 1996
Claims: 14
A superscalar processor in which multiple execution units are capable of performing at least an identical subset of operations. When an operation in a reservation station has been stalled for more than a predetermined number of cycles, it is rerouted to another execution unit capable of performing the operation instead of being bottlenecked.

5,649,137

Method and apparatus for store-into-instruction-stream detection and maintaining branch-prediction-cache consistency
Issued: July 15, 1997
Inventors: John G. Favor, et al
Assignee: AMD
Filed: January 3, 1996
Claims: 2
A processor updates instructions in a branch-prediction cache and also updates instructions recently provided to an instruction pipeline from the cache when an instruction being executed attempts to change the instructions.

5,649,136

Processor structure and method for maintaining and restoring precise state at any instruction boundary
Issued: July 15, 1997
Inventors: Gene W. Shen, et al
Assignee: HaL Computer
Filed: June 7, 1995
Claims: 18
A processor with speculative execution includes checkpoint hardware for scheduling instructions while maintaining and restoring precise state at any instruction boundary.

5,644,759

Apparatus and method for processing a jump instruction preceded by a skip instruction
Issued: July 1, 1997
Inventors: Gary J. Lucas, et al
Assignee: Unisys
Filed: January 19, 1995
Claims: 10
A system for instruction-fetch prediction. When a jump instruction is encountered, the preceding instruction is considered in predicting the next instruction. If the preceding instruction is a skip instruction, the result of evaluating a condition specified by the skip instruction is used in predicting the next instruction.

5,644,746

Data processing apparatus with improved mechanism for executing register-to-register transfer instructions
Issued: July 1, 1997
Inventors: Nicholas Peter Holt, et al
Assignee: ICL
Filed: April 30, 1992
Claims: 3
A processor that renames logical destinations onto physical destinations and implements at least one MOVE instruction to move data from a logical register source to a renamed destination.

5,644,741

Processor with single-clock decode architecture employing single microROM
Issued: July 1, 1997
Inventors: Mark W. Bluhm, et al
Assignee: Cyrix
Filed: October 18, 1993
Claims: 13
A microprogrammed processor with a decoder that detects the microaddress of a single-cycle macroinstruction during an input to the microcode store and before the microinstruction is read. The result of the detection is used to reduce the delay in fetching the next macroinstruction.

5,642,523

Microprocessor with variable-size register windowing
Issued: June 24, 1997
Inventor: Kenji Sakaue
Assignee: Toshiba
Filed: August 9, 1994
Claims: 19
A RISC processor that detects the registers used in a procedure call by number. A register window, which is used by the procedure, is saved and restored. The window for each procedure is dynamically determined by the highest register number actually used by the respective procedure.

OTHER ISSUED PATENTS

5,644,744 *Superscalar instruction pipeline having boundary-identification logic for variable-length instructions* M