by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,687,349

Data processor with branch-target-address cache and subroutine-return-address cache and method of operation
Issued: November 11, 1997
Inventor: Ralph C. McGarity
Assignee: Motorola
Filed: September 23, 1996
Claims: 4
A processor with a branch-and-link address cache (BLAC) and a branch-target-address cache (BTAC). The BLAC buffers corresponding subroutine call and return instructions. On the second call to a subroutine, logic stores the return instruction and the return address in the BTAC. The processor is therefore able to predict the target address of a subroutine return instruction similarly to the way it predicts the target address of branch instructions.

5,692,167

Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor
Issued: November 25, 1997
Inventors: Edward T. Grochowski, et al
Assignee: Intel
Filed: August 19, 1996
Claims: 15
A method of executing pipelined instructions in a processor that can write into the instruction stream. Data is written to memory in program order. The write address is compared to the address of each instruction in the pipeline subsequent to the write instruction. If there is a match, all subsequent instructions are flushed, refetched, and redecoded.

5,685,009

Shared floating-point registers and register port-pairing in a dual-architecture CPU
Issued: November 4, 1997
Inventors: James S. Blomgren, et al
Assignee: Exponential Technology (now S3)
Filed: November 29, 1995
Claims: 19
A dual-instruction-set CPU is capable of executing floating-point instructions. The CPU has an instruction decoder for each of two different instruction sets, and an execution unit and at least a floating-point status register in common for both.

5,687,337

Mixed-endian computer system
Issued: November 11, 1997
Inventors: Michael Joseph Carnevale, et al
Assignee: IBM
Filed: February 24, 1995
Claims: 10
A computer and methods in which a processor reads data, caches it, converts the endianness, and delivers the data to a requesting instruction, setting an indicator that the data has been converted.

5,689,720

High-performance superscalar-based computer system with out-of-order instruction execution
Issued: November 18, 1997
Inventors: Le Trong Nguyen, et al
Assignee: Seiko Epson
Filed: February 15, 1996
Claims: 11
A superscalar microprocessor and computer system with out-of-order instruction execution that includes a temporary register for storing speculative results.

5,692,170

Apparatus for detecting and executing traps in a superscalar processor
Issued: November 25, 1997
Inventor: David L. Isaman
Assignee: Metaflow
Filed: April 28, 1995
Claims: 11
In a superscalar processor, the decoder examines instructions stored in FIFO by the fetch stage to determine if any will cause a trap. When such an instruction is found, it and all younger instructions are flushed, and the fetcher begins fetching instructions from the trap handler.

5,692,169

Method and system for deferring exceptions generated during speculative execution
Issued: November 25, 1997
Inventors: Vinod K. Kathail, et al
Assignee: HP
Filed: October 18, 1994
Claims: 19
System and methods for executing instructions non-speculative instructions speculatively. The processor has a mode bit that determines whether it can speculatively execute non-speculative instructions. When in speculative mode, if a speculative exception is generated, the exception is deferred.