VOLUME 12, NUMBER 8
JUNE 22, 1998

MICROPROCESSOR REPORT

THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

Merced Slips to Mid-2000

Delay Jeopardizes Attempt to Gain Performance Lead

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Reality has reached out and tossed sand into the gears of Intel's product-development machinery. The company regretfully reported that an eight-month schedule slip has pushed the first volume shipments of its Merced processor from late 1999 to mid-2000. This slip will delay IA-64's penetration of the workstation and server markets and make it more difficult for Merced to achieve the performance lead, as Figure 1 shows. In the long term, however, the delay will probably have little effect on Intel's success in these markets.

Delay Caused by Poor Planning

Designing a new processor and a new instruction-set architecture (ISA) from scratch is always a long and daunting task. By pushing into the next decade, however, Intel's IA-64 effort is breaking two previous public commitments and is threatening to set a new record for gestation period.

The IA-64 effort was formally started in early 1994, when Intel and HP first began working together. The roots of this development effort stretch back even further, to research that HP and Intel had been separately conducting since 1991. When the partnership was announced (see MPR 6/20/94, p. 1), the partners said the first IA-64 products would ship before the end of the decade.

At the time, this statement seemed safe, as the internal plans were to complete the first IA-64 processor, code-named Merced, in 1998. Sources indicate that by 1996, however, the complexity of that chip was growing out of control, beyond what could be implemented in a 0.25-micron process. After examining and discarding proposals for a two-chip implementation, Intel decided to postpone Merced until its 0.18-micron process would be available. The new process allowed the design to be crammed onto a single chip. Unfortunately, this change delayed the ship date until mid-1999, when the new process would be ready.

Last fall, the company was confident enough in its progress to disclose the first details of the IA-64 instruction set (see MPR 10/27/97, p. 1) and reconfirm its commitment to 1999 shipments. At Microprocessor Forum, Intel's Fred Pollack promised that Merced would deliver "industry-leading performance" when it shipped. The design team at this point consisted of several hundred engineers, and the logical design was nearing completion.

Despite (or perhaps because of) this enormous staffing level, keeping the Merced program on schedule continued to be difficult. After a recent schedule review, senior management was shocked to discover that the chip was nowhere near tape out and in fact could not be expected to ship until the middle of 2000. Since Intel had publicly committed to 1999 shipments, it was forced to publicly acknowledge the change in plans.

Contrary to some rumors, the slip was not caused by delays in the 0.18-micron process; Intel still expects to ship 0.18-micron x86 products around 3Q99. Intel blames the latest delay in part on verification; it will take longer to test the design than originally thought. Given Intel's (and HP's) long experience in designing new processors and even new

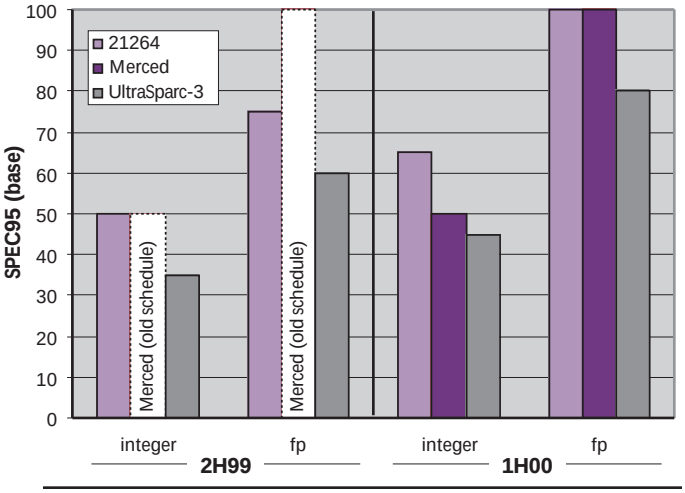

Figure 1. Merced had a good shot at gaining the performance lead in 2H99 on both integer and floating-point benchmarks, but by mid-2000 it could be merely among the pack in performance, particularly on the integer side. (Source: MDR estimates)

ISAs, however, this lack of foresight seems improbable. Other problems may exist with the design, but Intel is not willing to discuss them.

Competitive Performance May Suffer

Intel denies rumors that Merced is having trouble meeting its clock-speed and performance goals. Even if its performance is still on target, however, Merced will have more of a problem exceeding the competition than it would have had in 1999. Based on Moore's Law (a concept Intel should be familiar with), competitive performance should increase by about 25% during a six-month slip.

Our estimates support this assertion. We expect the fastest processor in 1999 will be the 0.25-micron 21264, delivering an estimated 50 SPECint95 and 75 SPECfp95, as Figure 1 shows. Had Merced been able to ship in that year, we believe it would have exceeded the Alpha chip's floating-point performance and potentially its integer performance as well, fulfilling Pollack's promise.

Part of Merced's performance comes from its use of 0.18-micron process technology, giving it an advantage over 0.25-micron processors. Under the previous plan, Merced was to be one of the first products off Intel's—or anyone else's—0.18-micron process. By mid-2000, however, 0.18-micron technology will be in common use for leading-edge microprocessors.

In particular, Intel is committed to delivering a 0.18-micron version of the 21264 processor to Digital as part of the two companies' foundry agreement (see MPR 11/17/97, p. 1). We expect that chip to reach 65 SPECint95 and 100 SPECfp95. Similarly, Sun's UltraSparc-3 (see MPR 10/27/97, p. 29) should also ship in a 0.18-micron process by that time, achieving 45 SPECint95 and 80 SPECfp95.

Since the schedule slip does little to improve Merced's performance, we expect it will have a tough time exceeding the integer performance of the 0.18-micron 21264. And its performance advantage over processors such as UltraSparc-3 and IBM's Power3 will be narrowed. Thus, Intel may not be able to claim bragging rights for its new architecture.

Sources indicate that Intel and HP are now pinning their performance hopes on the second-generation IA-64 processor, code-named McKinley. Intel had previously committed to delivering this device in 2001 with twice the performance of Merced in the same CMOS process. The company says the Merced slip will not affect McKinley, which is being developed by a separate design team.

Market Impact Delayed, Not Diminished

Even if Merced is not the fastest microprocessor in the world, its impact on the market won't be significantly diminished. The list of system vendors that have already committed to IA-64 is long and growing longer. It already includes Compaq, Data General, Dell, Digital, Groupe Bull, HP, Hitachi, IBM, ICL, Micron, NCR, NEC, Sequent, Siemens-Nixdorf, Silicon Graphics, Stratus, and Unisys. None of these companies is likely to reconsider its support of IA-64 because of this slip. With the backing of these companies, IA-64 has a clear path to taking over the majority of today's RISC-based workstation and server markets.

Of course, IA-64's impact will be delayed, and these vendors must make some tactical adjustments. Most base their current workstations and servers on Intel's Pentium Pro and Pentium II processors. These vendors will have to stay with the x86 line a bit longer before moving to Merced. Tanner (see MPR 3/9/98, p. 4), an x86 processor that plugs into the same Slot M as Merced, will allow system makers to develop and deploy Slot M systems that can later be upgraded to Merced. Given the latest slip, we expect Intel will develop a version of its Willamette x86 processor that also plugs into Slot M. This product could extend the company's x86 server line in 1H00.

Other vendors, such as HP and SGI, are moving from RISC to IA-64. HP is developing a processor called the PA-8700 to extend its current RISC line, tiding over customers until Merced systems are available. HP claims at least some of its PA-8700 systems will be upgradable to Merced. Similarly, SGI will rely on its forthcoming R14000 until Merced ships and will also offer upgradable systems. The delay will extend the current period of uncertainty for these vendors' customers, making them more vulnerable to poaching from non-IA-64 vendors such as Sun. But both HP and SGI are prepared to ride out the IA-64 delay.

A conspiracy theorist might claim Intel had this plan all along: prematurely announce the part to drive all competition from the market, then disclose the real schedule. Our sources indicate this schedule slip was a surprise at all levels of the organization, but the ultimate outcome is the same as in the conspiracy theory.

Financial Impact Minimal

The announcement of Merced's slip caused Intel's stock price to drop by 8%, but the financial markets seem to have overestimated Merced's impact on Intel's revenue. We had estimated Merced's 1999 revenue to be $400 million, less than 2% of the company's annual $25 billion revenue. With the new schedule, IA-64 is likely to contribute only a few percent to Intel's top line in 2000 and 5–10% in 2001. Not bad business if you can get it, but hardly enough to affect current stock prices.

Thus, the Merced delay is embarrassing for Intel but survivable. The company has much more pressing problems, like avoiding antitrust sanctions (see MPR 6/22/98, p. 8) and finding compelling applications that require the performance of a 400-MHz Pentium II, much less an 800-MHz Merced. Intel needs to get its scheduling problems under control, however, to prevent further slips in the future. M