CMOS Image Sensors Challenge CCDs

CMOS Makers in Search of the Holy Grail—the Digital Camera on a Chip

by Keith Diefendorff

Today, charge-coupled devices (CCDs) fill most of the sockets for digital image sensors in all types of devices. But CCDs have characteristics that make them less than ideal for inexpensive handheld devices. Several semiconductor manufacturers hope to exploit the power, size, and cost advantages of CMOS image sensors to capture the exploding market for sensors in digital video and still cameras.

Unlike CCDs, CMOS image sensors are built in standard CMOS semiconductor processes that are amenable to integrating analog and digital signal-processing circuits on the same die as the sensor array. In the past, CMOS image sensors have not been able to deliver image quality comparable to that of CCDs. But new developments, especially active-pixel-sensor technology, eliminate this shortcoming.

Issues remain, but it is now apparent that CMOS image sensors will displace CCDs in consumer-grade digital cameras. Fax machines, scanners, automobile-vision systems, and other devices will likely go the same way, as the issues are similar. In this article, however, we focus primarily on the most interesting opportunity for semiconductor manufacturers—the digital-camera market. Future Image and IDC, in their *Digital Camera Market Review and Forecast*, estimate the worldwide market for digital still cameras alone will be 8.5 million units by 2001.

Recognizing a new business opportunity in the digital-imaging market and the potential for it to boost demand for high-performance PC microprocessors, Intel has established a digital-video and imaging division that will market digital cameras for PCs using CMOS image sensors that Intel itself manufactures. TI, Motorola, Toshiba, Rockwell, and others also have their sights set on this emerging market.

Converting Photons Into Bits

Figure 1 shows the process of going from an optical image to a digital one. First, the optical image is focused on a digital image sensor. The image sensor comprises a rectangular matrix of light-sensitive elements, each of which represent one pixel of the image.

The number of pixels in the sensor array determines the resolution of the final image. On the low end, arrays of 320 × 240 pixels are adequate for NTSC video. Arrays of 640 × 480 are used for low-cost digital cameras and Web publishing. High-end cameras need at least 1,000 × 800 resolution, but these are already moving into the mainstream. The attention is now on 1,300 × 1,000 arrays, which begin to make digital cameras interesting alternatives to film-based snapshot cameras in the consumer market.

Each light sensor in the array is a photodetector that converts photons impinging on it to an electric charge via the photoelectric effect. The charge is integrated over a period of time long enough to collect a detectable amount of charge but short enough to avoid saturating the storage elements. This period is analogous to film exposure time. In general, photodetectors are more sensitive to light than film, which allows digital cameras to have short exposure times ranging from $^1/_{50}$ to $^1/_{10,000}$ of a second.

After the charge has been collected, it is transferred out of the array, where it is converted to a voltage proportional to the magnitude of the charge. Analog signal-conditioning circuits amplify and filter the signal, which is weak (a few millivolts in low light) and susceptible to noise injection. The signal-to-noise ratio (SNR) at this point is extremely important to the quality of the final image. A 42-dB SNRs is needed for a VHS-quality still picture. Typical CCD sensors today achieve SNRs better than 60 dB.

After conditioning, the analog signals are digitized by an analog-to-digital converter (ADC) into binary values that are proportional to the intensity of the light impinging on the respective sensors. The ADCs usually have a range of 8 to 10 bits, to cover the entire dynamic range of the signal. Subsequent processing is performed in the digital domain.

Unfortunately, photodetectors are monochromatic, so the digital image at this point is only grayscale. For creating a color image, a popular method is to print a polyimide mask of color filters over sensors in the array. A mosaic of red, blue, and two green filters is often used, arranged in a Bayer

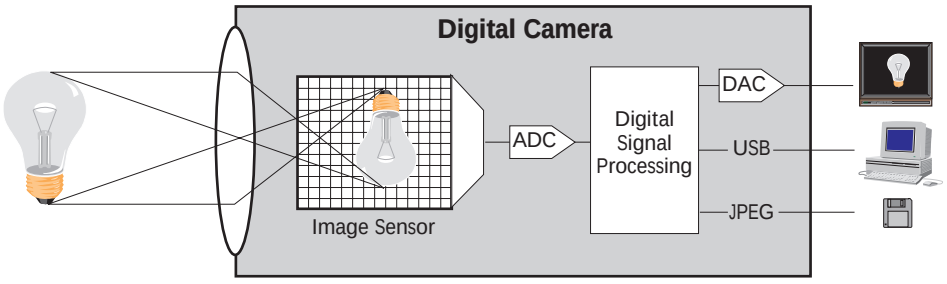

Figure 1. In a digital camera, the image is focused on an image sensor made up of an array of light-sensitive elements (pixels). Analog signals corresponding to the intensity of light falling on each pixel are converted to digital values by the ADC and processed into a final color image by digital-signal-processing circuits.

checkerboard pattern (two green filters due to the eye's greater sensitivity to green light). Then, a digital signal processor interpolates the intensity values of adjacent sensors to construct an RGB color estimate for each pixel in the image.

After the image is colorized, the digital signal processor performs additional functions to create the final image. These functions include exposure correction, removal of residual distortions from the lens system, image enhancement, white balancing (to correct for various light temperatures), and gamma correction (to match the linear response of the sensors to the logarithmic response of the eye).

Other functions necessary to implement a complete camera system include autofocus, image sharpening, electronic pan and zoom, image compression (e.g., JPEG), and communication of the image to the camera's memory, an LCD screen, a PC, or a television.

CCDs Provide Best Images

The first digital image sensors on the scene were charge-coupled devices (CCDs). CCDs operate by collecting charge generated by the photoelectric effect in a buried-channel MOS capacitor. A CCD pixel is formed by multiple gates, as Figure 2 shows, that are held at different voltages to create a potential well for collecting charge.

To read data in the sensor array, carefully timed clock signals are applied to the gates to march the charge from one pixel to another down the array—hence the name charge-coupled device. As a row of pixels is shifted out of the array, the charges are dumped into an analog shift register and shifted out serially to be converted to a voltage signal.

In a CCD, most of the silicon area is devoted to photon collection. The high fill factor (the ratio of photosensitive area to pixel size) gives CCDs good photoelectric efficiency. The FET structure and semiconductor process used for CCDs are designed to make good capacitors, maximize SNR, and achieve high charge-transfer efficiency (up to 99.999%). Achieving these goals requires a specialized process with large voltage swings and multiple supply and bias voltages.

A CCD's high photoelectric efficiency permits pixels to be packed tightly, producing high-resolution arrays on reasonably sized die. Today's megapixel CCDs typically use 4- to 5-micron pixel pitches on 0.5-inch square die (160 mm^2).

While CCDs have good efficiency, they do not scale well with technology. The minimum size of the pixel is dictated by the area required to collect photons and the diffraction limits of the optical system, not by circuit feature sizes. Improvements in process technology can boost photoelectric efficiency, allowing the pixel to shrink somewhat. But these improvements are more gradual than the square-law improvements we expect from process shrinks.

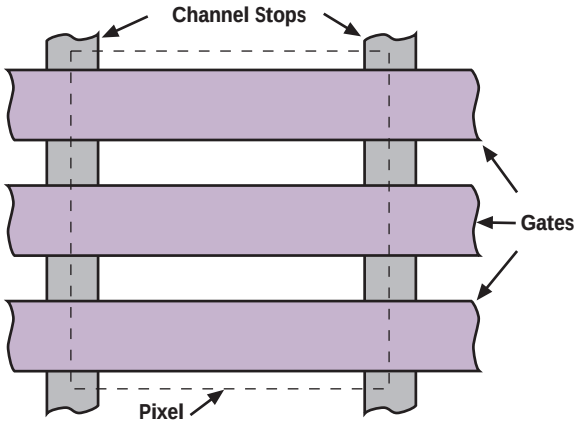

Figure 2. In a CCD, photons striking the pixel are converted to charge by the photoelectric effect and stored in the depletion-region beneath the gates formed by the gate potentials. These charges can be transferred from pixel to pixel down the array by modulating the gate voltages with carefully timed clock pulses. Channel stops isolate pixels in one column from those in the next.

CMOS Image Sensors Use Active Pixels

Unfortunately, the very architecture that makes CCDs efficient also makes them expensive. Their FET structure is incompatible with modern CMOS VLSI processes. As a result, CCDs cannot take advantage of the industry's massive CMOS fabrication infrastructure. The CCD process is complex and thus suffers from poor yields, further increasing costs.

Using pure-CMOS to overcome the shortcomings of CCDs is not a new idea. But a narrow dynamic range and high noise levels have plagued CMOS sensors until recently.

Early CMOS sensors used a passive-pixel structure (PPS). In this arrangement, a photodiode is paired with a transistor switch, as Figure 3 shows, to dump the accumulated charge onto a column bus. This structure has advantages over CCDs in that the array can be X-Y addressed and read out a row at a time. This method lowers the analog bandwidth requirement compared with the serial readout of CCDs, reducing susceptibility to noise injection. But the extra transistor takes up space, which lowers the fill factor and gives PPS sensors lower efficiency and SNR than CCDs.

Recently, however, CMOS scaling has made transistors small enough that an amplifier can be included at every pixel. Although the amplifier takes area and reduces the fill factor even further, the amplification more than compensates. This active-pixel-sensor (APS) technology raises the SNR and efficiency of CMOS image sensors near those of CCDs, bringing image quality above the threshold necessary to serve the consumer digital-camera market.

Although CMOS photodetectors do not scale any better than CCD photodetectors, CMOS pixels will scale better than CCD pixels. As CMOS transistors shrink, additional active circuitry can be placed at each pixel sensor. With 0.18- and 0.13-micron technology, each pixel can include multistage amplifiers, ADCs, and even digital signal processing. Such circuitry can increase sensitivity and reduce noise, allowing the pixel to shrink. The overall pixel will still not shrink at the rate of normal CMOS circuitry, but it will scale better than its CCD counterpart.

CMOS Allows Integration

With image-quality problems licked, the integration, power, and cost advantages of CMOS come into play. With CMOS, unlike CCDs, the ADCs can be integrated onto the die, close to the sensor array. This design reduces the analog signal's susceptibility to noise and makes the output of the chip fully digital. CMOS also makes it possible to integrate on a chip digital signal processing and other functions necessary to produce a complete digital camera.

CMOS sensors require less power than CCDs. They operate on a single low-voltage supply. (On-chip bias generators can provide different voltages for the sensors or ADCs if necessary.) All clock signals can be generated and contained on chip, and all off-chip communication is fully digital. The net effect is dramatically lower system power requirements than CCDs—a big plus for battery-powered cameras.

CMOS sensors also beat CCDs in manufacturing costs. Standard CMOS processing allows CMOS sensors to take advantage of the enormous infrastructure and learning curve of the semiconductor industry. CMOS sensor processes are simpler than CCD processes, giving them higher yields. This yield becomes especially important as the arrays are scaled to higher resolutions. CMOS sensors are also less susceptible to defects. A defect may affect only a single pixel in a CMOS sensor, whereas in a CCD, a similar defect would wipe out an entire column. These factors make CMOS image sensors more manufacturable than CCDs.

CMOS sensors should ultimately have a price advantage over CCDs as well. Today, there are about five large manufacturers of CCDs. With CMOS sensors, anyone with a 0.35-micron fab can—and probably will—get into the market. The competition from many vendors should drive prices down.

Recently, prices of CCDs have fallen dramatically, driven down by the competitive threat from CMOS sensors. Low-end 320 × 240 CCDs are now available in the $12 to $35 range, and 640 × 480 versions have dropped below $80 (plus another $10 for external electronics). CMOS sensors are already slightly less costly than CCDs at these resolutions.

High-end 1,000 × 1,000 CCDs capable of 30 fps are still pricey at over $500, but these will be coming down as manufacturers struggle to squeeze every last drop of return out of their CCD investments. Because of their better yields, CMOS sensors are expected to be far less expensive than CCDs at these higher resolutions. Eventually, the manufacturing cost advantages of CMOS will become overwhelming, and CCDs will be unable to keep up the pace.

Several Companies Making CMOS Sensors

Today, there are relatively few CMOS sensors on the market, but there is an enormous amount of activity, and we expect a continuous stream of new announcements. Unfortunately, details of many of the upcoming sensors are unknown at this time. Table 1 presents a representative sampling of recent activity.

Intel sells the 971 PC Camera Kit, which contains its own 768 × 576-pixel CMOS APS sensor. The 80971AC is built in the company's standard 0.35-micron P854 process. Sources in the imaging industry believe that Intel's sensor technology was developed by Photobit (La Crescenta, Calif.). Although neither company acknowledges this relationship, it seems likely that Intel would try to leverage existing technology rather than develop new technology itself.

Intel has announced a major initiative with Kodak to jointly develop imaging products. The agreement includes a broad patent cross-license. The companies agreed to spend $150 million over three years to promote their imaging products. Sources indicate that image sensors are not part of the Intel-Kodak agreement.

Kodak has, however, teamed up with Motorola to build image sensors based on technology it calls ImageMOS. Photobit is the source of that technology and is also the design house for Kodak-Motorola sensors. Kodak says it has several cameras using this technology on the drawing boards.

Photobit was spun out of NASA's Jet Propulsion Lab (JPL) in 1995 with an exclusive license to JPL's APS technology from Caltech. At Hot Chips last year, Photobit described its APS technology in conjunction with a 512 × 384-pixel

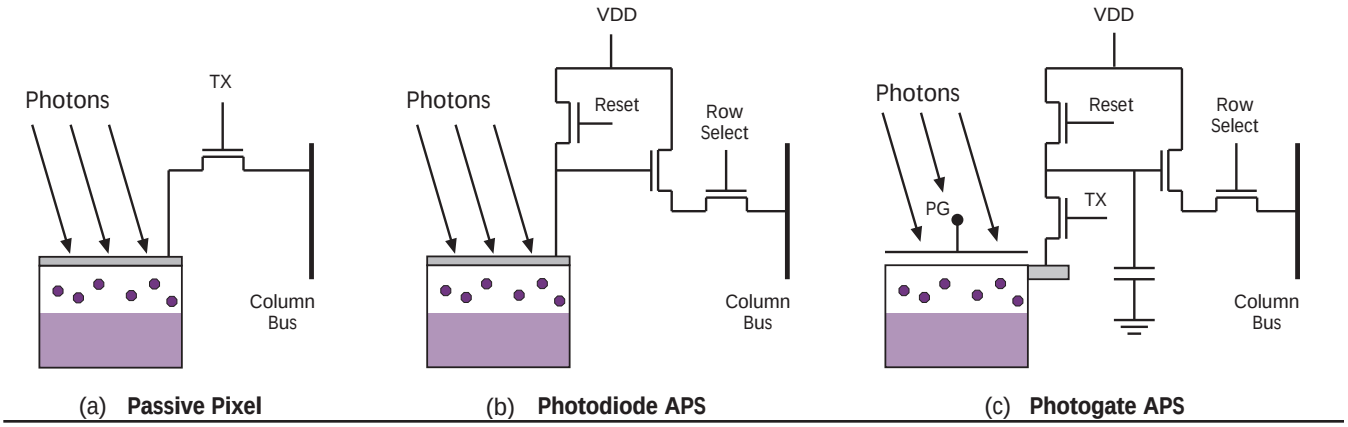

Figure 3. Early CMOS image sensors used a passive-pixel arrangement. But CMOS scaling now allows active pixels, which have amplifiers at each pixel site to improve the light sensitivity and signal-to-noise ratio.

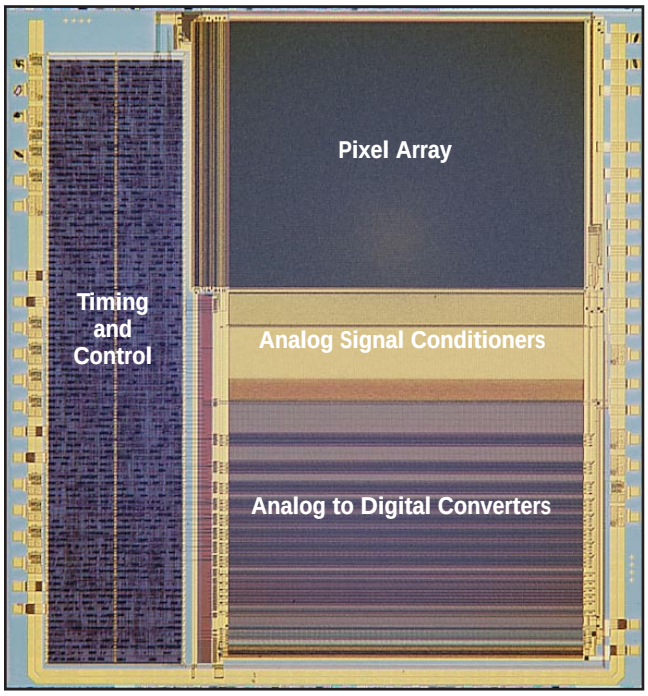

Figure 4. Photobit's PB159 CMOS image sensor is 8.6 × 9.4 mm with 196,608 (512 × 384) active pixels and column-parallel analog-to-digital converters. Each pixel is 7.9 × 7.9 microns.

APS. Figure 4 shows the PB159, which uses a pixel consisting of a photodiode and three transistors similar to the design in Figure 3(b). The PB159 integrates 8-bit column-parallel ADCs, automatic exposure logic, windowing, and an I^2C serial command interface. Presumably, it is similar to the technology employed in the Kodak, Motorola, and Intel sensors. Photobit also has a 1,280 × 1,024 CMOS APS with an on-chip 10-bit ADC that is capable of 60 fps.

Rockwell Semiconductor has introduced five devices ranging from 352 × 288 pixels (CIF resolution) to 960 × 720 pixels. The Ri0352A, 640A, 800A, and 960A all have APS, while the Ri0352P does not. The sensors all integrate signal-conditioning circuits, a 10-bit ADC, and a digital video interface capable of 30 fps. There are rumors that the Rockwell technology may also be based on Photobit's. Prices for the Rockwell sensors range from $18 to $63.

A unique feature of the Rockwell sensors is "microlenses." These are 0.5- to 0.8-micron glass beads that concentrate light onto the detectors and raise the SNR to 46 dB. We expect microlenses to be a feature of many of the new sensors coming from other manufacturers.

VLSI Vision (Edinburgh, Scotland) supplies a 1,000 × 800-pixel CMOS APS to Sound Vision (Framingham, Mass.) for its SVmini-2 camera, which is marketed by Vivitar and Umax. Both of these cameras sell for around $400. At ISSCC98, the company described a more interesting 306 × 244-pixel single-chip NTSC video camera that includes a 300-MOPS dataflow processor to perform signal processing. The 68-mm^2 chip uses a 12 × 11-micron pixel and is implemented in 0.8-micron double-layer-metal CMOS. VLSI Vision said that with microlenses, low-power design techniques, process improvements, and a process shrink, it plans to get the SNR up to 57 dB (from 45 dB currently).

Texas Instruments announced it will sample the TC286 640 × 480-pixel image sensor in July. TI, a major supplier of CCDs, claims its CMOS sensor has image quality comparable to that of CCDs. In future chips, TI plans to integrate ADCs, digital signal processing, and image compression.

Toshiba has demonstrated a prototype 1.3-million-pixel CMOS APS that meets the requirement of the 1,280 × 1,024 SXGA format. The die measures 144 mm^2 in 0.6-micron triple-poly double-level-metal CMOS and uses a pixel size of 5.6 × 5.6 microns. The triple-poly process is more complex than what other manufacturers are using but may be responsible for the device's small pixel size. At ISSCC this year, the company said it had further reduced the pixel size to just 3.7 × 3.7 microns in the same process.

Other Designs in Progress

AT&T Bell Labs (now Lucent Technologies) also entered into a technology agreement with Photobit. The company recently described a 354 × 292-pixel single-chip digital camera based on a five-transistor photogate APS shown in Figure 3(c). Color reconstruction and gamma correction are performed with 100 MOPS of on-chip digital signal processing.

Atmel and Polaroid have joined forces to develop CMOS image sensors that will integrate analog signal-conditioning circuits, DSPs, and flash memory. Hyundai Electronics has developed an XGA resolution (1024 × 768) CMOS sensor with integrated 6-bit automatic gain control and 8.5-bit ADC.

CMOS APS Device	Process µm	Process Poly/Met	Resolution	Pixel µm	SNR dB	ADC bits	Integration	Rate fps	Power mW	Power Volts	Comments
VLSI Vision	0.8	1P2M	306 x 244	12 x 11	45	10	300 MOPS DSP	30	550	5	Camera on a chip
Bell Labs, Lucent	0.8	1P2M	354 x 292	18 x 18	n/a	8	100 MOPS DSP	30	182	3.3	Shown at ISSCC98
Photobit PB159	0.5	2P3M	512 x 384	7.9 x 7.9	60	8	Autoexposure	30	50	5	Column-parallel ADCs
Intel	0.35	854	768 x 576	n/a	n/a	n/a	n/a	still	n/a	n/a	In 971 PC Camera Kit
Rockwell Ri0960A	n/a	n/a	960 x 720	n/a	46	10	Serial I/F	30	100	3.3	Uses microlenses
VLSI Vision	0.8	1P2M	1000 x 800	10.5 x 10.5	64	12	None	5	100	5	SVmini-2 camera
Photobit PB720	0.5	2P3M	1280 x 720	7.9 x 7.9	60	10	Windowing	60	250	5	
Toshiba	0.6	3P2M	1318 x 1030	5.6 x 5.6*	n/a	n/a	n/a	still	30	3.3	* 3.7 x 3.7 at ISSCC98

Table 1. Nearly all recent CMOS image sensors use active-pixel sensors. New development activity seems to be focused on higher resolution, better SNR (image quality), and higher levels of integration.

New Ideas Abound

G-Link (Santa Clara, Calif.), through a partnership with the Institute for Microelectronics Stuttgart (IMS), is developing CMOS sensors based on that company's high-dynamic-range CMOS (HDRC) technology. HDRC delivers 120 dB of dynamic range using a logarithmic pixel-compression technology. This technology eliminates the need for shutters, aperture control, automatic gain control, and gamma correction. G-Link has wafer supply contracts with Chartered Semiconductor and TSMC. It also plans to build SVGA sensors in IBM's 0.35-micron CMOS process.

Amain Electronics (Simi Valley, Calif.), a developer of specialized infrared image sensors, has a unique continuous-modulation scheme for reading data from the array. Instead of dumping all the collected charge at once, as most APS devices do, the charge in the well is continuously sampled. Between sampling operations, a fixed amount of charge is switched into a subtraction capacitor. Amain says this approach, along with its oversampled sigma-delta ADC, has a smoothing effect that reduces noise.

Stanford University's Image Sensor Group has demonstrated pixel-level ADC. In this approach, an analog-to-digital converter is placed at every pixel. Each ADC uses very little power, because it has to run at only a few kilohertz. Since all analog signals are confined to the vicinity of the pixel, noise is reduced. Another advantage of this approach is scalability; the same pixel can be used for arrays of any size. The ADC requires more area than an APS amplifier, but Stanford has demonstrated a 9 × 9-micron pixel in 0.35-micron technology with a good (25%) fill factor. Both HP and Intel have built test chips.

The IMEC research center in Leuven, Belgium, is developing a technology that uses special p+ doping to create an electrostatic barrier around the pixel. The barrier funnels carriers generated anywhere in the pixel area into the junction that is accumulating charge. This technique should raise the sensitivity of CMOS sensors close to that of CCDs.

CCDs to Fade Away

CMOS image sensors will not eliminate CCDs soon. CCDs still produce higher-quality and higher-resolution images, and that will likely remain true until support for CCD research finally dries up. The industry has 25 years of experience manufacturing and using CCDs, whereas CMOS sensors have become viable only in the past three or four years. CCD development continues: Sony, Matsushita, NEC, and TI have all recently announced new megapixel CCD sensors.

But the CMOS sensors coming onto the market now are every bit as good as CCDs at the low end. Nearly all the CMOS sensor manufacturers have on the drawing boards megapixel versions that will rival the best CCDs in resolution and image quality within the next two to three years.

The advantages of CMOS image sensors over CCDs seem compelling. Standard CMOS processes have lower wafer cost and better yields. As competition heats up—which is bound to happen, since CMOS sensors can be built by just about anyone—prices may drop even faster than costs. Integration of other circuits on the same die as the sensor array has obvious advantages in power, space, and system-level costs. By Photobit's estimates, CMOS APS sensors need 1% of the system power and 10% of the physical volume of CCDs with comparable image quality.

As CMOS geometries shrink, integration of digital processing horsepower, at each pixel or next to the sensor array, will offer capabilities beyond that possible with CCDs. Near-35-mm-film resolution and MPEG2-encoded HDTV video should be available in a few years from a single chip in your PDA. On-chip DSPs performing billions of operations per second will eliminate exposure, focus, stability, and lens-distortion problems, making good photographers out of rank amateurs.

Intel sees digital imaging as a MIPS-intensive application that can showcase its high-performance microprocessors and drive demand for PCs. But beyond that, its establishment of a full division with profit-and-loss responsibility indicates that it also sees digital imaging as a big business in and of itself. Intel wants to be a vertical supplier to this market, providing sensors, microprocessors (e.g., StrongARM), ASICs, and flash memory. CMOS sensors provide a vehicle for putting aging fabs to good use, and Intel is betting heavily on them in its bid for this market. Intel's presence alone should make CCD manufacturers nervous.

Today, CCDs still deliver superior image quality over CMOS image sensors. This will remain true for many years in applications where power, space, and cost are not issues. So if you need a cryogenically cooled infrared sensor for your space telescope, look to CCDs—otherwise, your best bet will be a CMOS image sensor. M

For More Information

For more information on CCDs or CMOS image sensors, access the following Web sites:

- Intel, *www.intel.com/imaging*
- Photobit, *www.photobit.com*
- Motorola, *mot2.indirect.com/adc/markets/image.html*
- Rockwell, *www.nb.rockwell.com/platforms/personal_imaging/*
- TI, *www.ti.com/sc/docs/disp/disp.htm*
- G-Link, *www.glinktech.com*
- VLSI Vision, *www.vvl.co.uk/*
- Stanford Image Sensor Group, *www-isl.stanford.edu/people/dyang/imaging.shtml*
- Sony, *www.sel.sony.com/semi/ccdarea.html*