by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,701,508

Executing different instructions that cause different data-type operations to be performed on single logical register file
Issued: December 23, 1997
Inventors: Andrew F. Glew, et al
Assignee: Intel
Filed: December 19, 1995
Claims: 35
Methods for executing different instruction sets (e.g., MMX and floating point) on a processor in a register file. A data processor executes a first set of instructions of a first instruction type (e.g., MMX) on what at least logically appears as a single logical register file. To these instructions, the single logical register file appears to be a flat register file. Additionally, the processor executes a second instruction type (e.g., floating point) using the logical register file, where the register file is treated as a stack.

5,701,442

Method of modifying an instruction-set architecture of a computer processor to maintain backward compatibility
Issued: December 23, 1997
Inventors: Ronny Ronen
Assignee: Intel
Filed: September 19, 1995
Claims: 13
A processor architecture's instruction set has preallocated "hintable" NOP instructions. These NOP instructions have no architectural significance. In current-generation processors, these NOPs may have no function. In future-generation processors, however, these "hintable" NOPs may be used, in a backward-compatible manner, to provide microarchitectural hints, such as caching or power hints, to the processor.

5,701,425

Data processor with functional register and data-processing method
Issued: December 23, 1997
Inventor: Shigeru Nakahara
Assignee: Hitachi
Filed: August 28, 1996
Claims: 24
A processor, with instructions having an opcode and an operand, has general-purpose and functional registers. The functional registers have preassigned functions associated with them (e.g., logical NOT), such that the predefined function of a register is performed when data is written to or read from them.

5,699,536

Computer processing system employing dynamic instruction formatting
Issued: December 16, 1997
Inventors: Martin Edward Hopkins, et al
Assignee: IBM
Filed: April 13, 1995
Claims: 46
A processor with a method of superscalar issue, internally similar to VLIW, whereby instructions of the instruction set may be sequentially scheduled to an execution unit. In parallel with the sequential scheduler, instructions are fetched and group-formatted in the processor into "long decoded instructions" (LDIs). Each LDI is issued to multiple second execution units in parallel.

5,696,958

Method and apparatus for reducing delays following the execution of a branch instruction in an instruction pipeline
Issued: December 9, 1997
Inventors: Todd C. Mowry, et al
Assignee: Silicon Graphics
Filed: March 15, 1995
Claims: 20
A pipelined processor with conditional branch instructions. For every branch instruction, the instruction-fetch stage begins fetching both the branch target and the next sequential instruction before the execution unit completes processing the branch instruction.

5,696,956

Dynamically programmable reduced-instruction-set computer with programmable processor loading on program-number-field and program-number-register contents
Issued: December 9, 1997
Inventors: Rahul Razdan, et al
Assignee: Digital
Filed:November 9, 1995
Claims: 6
A PRISC computer with two types of instructions is claimed. One type is a standard RISC type. The other type is specialized for specific applications. The second instruction type comprises a sequence of RISC-like instructions that are precompiled into single instructions, which are then loaded into a programmable functional unit for execution in a single cycle. M