IBM Copies TI's 'C54x DSP

Reverse-Engineered Core the Latest Addition to ASIC Library

by Jim Turley

IBM has paid the sincerest form of flattery to Texas Instruments by announcing the culmination of its two-year project to copy TI's popular 'C54x DSP processor core. IBM's reverse-engineered core design is already sampling in the form of two standalone DSP chips, but IBM's real strategy is to procure ASIC design wins in the booming wireless market, where TI's 'C54x family reigns supreme.

The addition of the C54x DSP core is another step in IBM's strategic shift away from standard microprocessor products and toward becoming a full-line ASIC supplier. The company's recent acquisition of the ARM7 (see MPR 3/30/98, p. 8) and picoJava (see MPR 3/30/98, p. 8) cores, along with the recent shift away from Somerset's standard parts (see MPR 6/22/98, p. 10), all emphasize the move toward an ASIC business.

IBM's DSP a Cycle-Accurate Copy of TI's

In a nutshell, IBM's new DSP core is a fully compatible duplicate of TI's TMS320C54x family of DSP chips. To avoid any confusion, IBM calls its core C54xDSP. IBM claims the two families are completely binary compatible, down to cycle-by-cycle timing of individual instructions and operations. This level of accuracy should allow developers to swap existing binary code between the TI and IBM versions of the chip with no discernable differences in performance or execution.

The level of compatibility is such that IBM saw no need to develop its own design tools for its C54x family. Customers can simply use existing compilers, assemblers, linkers, and debuggers developed for TI's 'C54x family. TI has recently altered the fine print in its software-licensing agreements to specifically forbid their use with non-TI silicon, apparently in anticipation of IBM's move.

Already sampling are two versions of the chip: IBM's C541 and C547 devices, which are pin-compatible with their TI namesakes. IBM builds its devices in its 0.25-micron SA-12 process in Vermont. The tight process geometry forces a move to a lower supply voltage than TI uses for its chips. IBM covers this difference by building voltage regulation onto the die, so the DSP core can run at 2.2 V (nominal) while maintaining socket compatibility with the 3.3-V TI parts.

As a slight differentiator from TI, IBM will also offer its chips with split power supplies and allow customers to separate the core supply from the I/O supply. For new designs that are not constrained by socket compatibility, this option will allow users to reduce the chip's overall power consumption somewhat by taking advantage of the lower core voltage. IBM has characterized the part with core voltages as low as 1.65 V.

At that low voltage, the C541 and C547 can run at 40 MHz. Raising the core voltage to 2.3 V gets the frequency to 55 MHz, which is about 15% slower than TI's top speed of 66 MHz for the same part. IBM believes that its customers are more concerned with power consumption than peak performance, so the lower ceiling shouldn't be a problem in battery-powered wireless applications. For cellular handsets, 40–50 MHz is ample, so IBM's conservative clocking should not present any market problems.

Legal Ground Seems to Be Covered

IBM also foresees no problems on the legal front. Like Lexra (see MPR 2/16/98, p. 13), IBM believes its clean-room design infringes no TI intellectual property. Which is not to say that IBM's DSP core doesn't make use of TI patents—only that IBM is covered by the appropriate cross-licenses to make the endeavor legally tenable. So far, IBM has reported no overtures from TI's legal department.

The C54x is not the first core IBM has reverse engineered. The company's 80186 and '196 cores were also clean-room implementations, although they were not necessarily as cycle-accurate as the C54x copy. IBM no longer promotes these 16-bit cores for its ASIC library. The company also downplays MWave (see MPR 12/9/92, p. 1), its media processor that has since fallen out of favor.

ASIC Tape Out in 4Q98

Although the C541 and C547 DSP chips have been sampling since late last year, the version of the core for ASIC integration is still in the last stages of design. IBM expects the core design to be complete in 3Q98 and the first C54x-based ASIC should tape out in 4Q98. That schedule should put the first samples of C54x-based parts at around the middle of 1999. As with most ASIC vendors, IBM is not naming the customers for its ASIC core, allowing them to identify themselves.

As IBM continues its march toward becoming a major ASIC house, its inevitable that it will acquire more and more cores. It was also inevitable that it would acquire at least one DSP, and TI's 'C54x was an obvious and juicy target. M

Price & Availability

IBM's C541 and C547 DSP processors are in production now; no pricing information has been released. The ASIC core will be ready for designs in 3Q98. For more information, contact IBM at 802.769.6231 or set your browser to *www.chips.ibm.com/products/asics.*