AUDIO/VIDEO

Compression puts images on a diet. Advanced compression techniques minimize storage density and transmission bandwidth for still and video images. Brian Dipert, *EDN*, 6/18/98, p. 71, 11 pp.

Parallel video servers: A tutorial. This article introduces a framework for the design of parallel video server architectures and addresses three central architectural issues: video distribution architectures, server striping policies, and video delivery protocols. Jack Lee, Chinese University of Hong Kong; *IEEE Multimedia*, 6/98, p. 33, 9 pp.

BUSES

Special report: Much ado about CompactPCI. What does the crystal ball reveal for the future of CompactPCI? Will the standard soar with the eagles or sink like a certain well-known ocean vessel? Jerome Krasner, *Embedded Systems Programming*, 6/98, p. 84, 6 pp.

The VMEbus celebrates its sweet 16 birthday as strong as ever. In the face of competition, the VMEbus has implemented a host of "speed-ups" to keep pace, with no end in sight. Richard Nass, *Embedded Systems Development*, 5/98, p. 10, 4 pp.

Low-voltage differential signaling reports for bus duty. Based on point-to-point LVDS technology, bus devices combine speed, low power, and low noise. Jeff Child, *Electronic Design*, 5/25/98, p. 39, 3 pp.

DEVELOPMENT TOOLS

Software development tools break down integration challenges. Software tools progress to meet the needs of a plethora of embedded designs from cruise missiles to luxury cars. Teri Sprackland, *Electronic Design*, 6/25/98, p. 53, 5 pp.

In-circuit emulation faces the challenge of system complexity. To see inside today's dense system-on-a-chip designs, traditional in-circuit emulators are forced to learn new tricks and rely on facilities supplied by the silicon. Tom Williams, *Embedded Systems Development*, 5/98, p. 47, 4 pp.

DSP

Suppliers tailor DSPs for digital motor control. Suppliers ready DSP solutions for consumer and industrial use by integrating peripherals, memory, and control functions around a core. Ashok Bindra, *Electronic Design*, 5/25/98, p. 73, 4 pp.

Higher-throughput DSP chips take on complex applications. Consumer, telecommunications, and instrumentation gain from DSP chips with reduced costs and lower power consumption. Dave Bursky, *Electronic Design*, 5/25/98, p. 80, 4 pp.

Optimize memory subsystem for top performance. A better understanding of memory accesses allows DSP memory subsystems to be better matched to the DSP chips. Richard Jaenicke and Paul Taddonio, Sky Computer; *Electronic Design*, 5/25/98, p. 90, 3 pp.

Factors to consider when choosing the right DSP for the job. DSP performance isn't just about MIPS. Application-specific issues can strongly affect a chip's performance. Ian Main, Spectrum Signal Processing; *Electronic Design*, 6/8/98, p. 67, 4 pp.

IC DESIGN

Multicore chips challenge system-on-chip designers. Combining high-speed digital-logic cores, memory arrays, and analog blocks amplifies the problems of chip-design decisions concerning tasks such as on-chip buses, testability, and system placement and routing. Jim Lipman, *EDN*, 6/18/98, p. 56, 7 pp.

Long overdue unified hardware/software codesign language comes to light. Today's system-on-chip (SoC) designer must master several languages and tools. A simple hardware/software (HW/SW) codesign language (CDL), hidden in common parts of the IEEE 1076 VHDL-93 and ANSI/ISO/IEC-8652:1995 Ada-9 standards, offers a viable and yet often-overlooked solution to this problem. Sy Wong, Cornell; *Electronic Design*, 5/13/98, p. 60, 2 pp.

MEMORY

The choice for future mainstream memory is clear. SLDRAM and Direct Rambus are locked in a race for DRAM technology dominance. SLDRAM has advantages over Direct Rambus, including a more robust system and lower manufacturing costs. Peter Gillingham, Mosaid Technologies; *Computer Design*, 6/98, p. 106, 2 pp.

PERIPHERAL CHIPS

Optimized ADCs pack major features on chip. Designers are pushing the performance of imaging and video systems to new heights. In addition, they are bringing digital processing solutions closer to the antenna. Ashok Bindra, *Electronic Design*, 5/13/98, p. 46, 5 pp.

Two-chip sets encourage GPS proliferation. As designs for Global Positioning System (GPS) satellite receivers improve and GPS capabilities proliferate, IC houses are moving toward ever higher levels of integration to enable cheap and ubiquitous GPS positioning. *Portable Design*, 6/98, p. 60, 2 pp.

PROCESSORS

M•Core poses challenge to ARM in low-power apps. Motorola's M•Core processor is posing a significant challenge to Advanced RISC Machines' Thumb architecture in the low-power applications arena. Robert Gott, *Computer Design*, 6/98, p. 14, 2 pp.

SYSTEM DESIGN

Power managing sub-3-V designs. As IC die sizes shrink and battery voltage drops, portable system power requirements continue to rise. Here's a look at why—and what you can do. Cheryll McKinnon, *Portable Design*, 6/98, p. 25, 6 pp.