by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,710,912

Method and apparatus for enabling a computer system to adjust for latency assumptions
Issued: January 20, 1998
Inventors: Michael S. Slansker, et al
Assignee: HP
Filed: May 6, 1993
Claims: 21
Methods and system that allow an object-code-compatible processor, which may have different function unit latencies than those for which the program was originally created, to execute properly.

5,708,841

Processor architecture providing speculative, out-of-order execution of instructions
Issued: January 13, 1998
Inventors: Valeri Popescu, et al
Assignee: Hyundai (via Metaflow)
Filed: September 17, 1996
Claims: 19
A superscalar, out-of-order microprocessor with register renaming. The microprocessor has branch prediction for conditional branches and in-order instruction retirement.

5,708,803

Data processor with cache memory
Issued: January 13, 1998
Inventors: Kouichi Ishimi, et al
Assignee: Mitsubishi
Filed: July 30, 1996
Claims: 4
A data processor that has a branch predictor that may or may not predict a branch. When the branch predictor predicts a branch, and the target of the branch is not in a cache, the memory interface is inhibited from initiating the target fetch until the branch prediction is confirmed.

5,706,491

Branch-processing unit with a return stack, including repair using pointers from different pipe stages
Issued: January 6, 1998
Inventor: Steven C. McMahan
Assignee: Cyrix
Filed: February 26, 1996
Claims: 6
A branch processing unit (BPU) in a superscalar x86 microprocessor. The BPU includes a return stack for call/returns, including return-stack-pointer repair in the case of the failure of a call/return to confirm (decode) or resolve.

5,706,483

Run-time code compiler for data block transfer
Issued: January 6, 1998
Inventors: Stuart Raymond Patrick, et al
Assignee: Microsoft
Filed: December 13, 1994
Claims: 25
Methods and apparatus for efficiently transferring a block of data from a source to a destination in the memory of a computer system. The method transfers data in multiple-byte words on word-aligned boundaries of memory as much as possible to reduce the number of fetches, writes, and memory cycles. Any unaligned first part is first transferred, then aligned words are transferred.

5,706,466

Von Neumann system with Harvard processor and instruction buffer
Issued: January 6, 1998
Inventor: Kenneth A. Dockser
Assignee: VLSI
Filed: January 13, 1995
Claims: 12
A Harvard-architecture processor with a combined data/instruction memory. A dual-port random-access instruction buffer between memory and the processor provides much of the enhancement of an instruction cache when used with a RISC instruction set, but at a much lower cost. The instruction buffer always holds the first requested instruction from memory in its first location, regardless of the alignment in memory.

5,706,459

Processor having a variable number of stages in a pipeline
Issued: January 6, 1998
Inventor: Sakurai Atsushi
Assignee: Fujitsu
Filed: December 30, 1994
Claims: 43
A pipelined processor that dynamically splits a memory-access pipeline stage into two stages: an address-generation stage and a data-access stage. The splitting allows continued processing of subsequent instructions while waiting for data.

OTHER ISSUED PATENTS

5,706,492 *Method and apparatus for implementing a set-associative branch target buffer* M