by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,732,235

Method and system for minimizing the number of cycles required to execute semantic routines
Issued: March 24, 1998
Inventors: James Allan Kahle, et al
Assignee: IBM
Filed: January 25, 1996
Claims: 10
In a processor emulating a target instruction set with a block of instructions of a native instruction set, the last instruction of a block of native instructions will branch to a routine to begin the next target instruction. Methods and hardware are provided that avoid execution of those branches by keeping a count of the native instructions in the block and forcing a branch when the count is reached.

5,732,210

Use of dynamic translation to provide fast debug event checks
Issued: March 24, 1998
Inventor: William B. Buzbee
Assignee: HP
Filed: March 15, 1996
Claims: 17
Dynamic translation is used during debugging of a computer application process. During runtime, the first application is dynamically translated to produce translated code. Debugging code, such as a conditional breakpoint, may then be added to the translated code.

5,729,760

System for providing first-type access to register if processor in first mode and second-type access to register if processor not in first mode
Issued: March 17, 1998
Inventor: David I. Poisner
Assignee: Intel
Filed: June 21, 1996
Claims: 18
A microprocessor operating in system-management mode is allowed different access to certain I/O-mapped registers than the access permitted to those registers in normal operation.

5,729,729

System for fast trap generation by creation of possible trap masks from early trap indicators and selecting one mask using late trap indicators
Issued: March 17, 1998
Inventor: Arthur T. Leung
Assignee: Sun
Filed: June 17, 1996
Claims: 20
In a pipelined superscalar processor, traps issued by the execution units occur at earlier or later times, based on the function of the execution unit. Trap masks are selected to correctly mask traps based on the issue sequence of instructions in the pipeline, preventing a subsequently issued early trap from occurring before a previously issued late trap.

5,727,177

Reorder buffer circuit accommodating special instructions operating on odd-width results
Issued: March 10, 1998
Inventors: Brian D. McMinn, et al
Assignee: AMD
Filed: March 29, 1996
Claims: 22
A reorder buffer in a processor that has a FIFO-like reorder buffer typically used to store and supply noncommitted results. The reorder buffer has a bit width for handling standard data types. For data types wider than the reorder buffer, the invention provides for an extended reorder-buffer entry.

5,724,566

Pipelined data processing including interrupts
Issued: March 3, 1998
Inventors: Gary L. Swoboda, et al
Assignee: Texas Instruments
Filed: October 31, 1996
Claims: 22
Method and hardware for handling interrupts in a pipelined processor. The processor keeps a record of the addresses of all instructions in the pipeline. In the event of an interrupt, the processor stops execution, saves the address in the program counter and the address of the previous instruction, handles the interrupt, and restores the two saved addresses.

5,724,533

High-performance instruction data path
Issued: March 3, 1998
Inventors: John S. Kuslak, et al
Assignee: Unisys
Filed: November 17, 1995
Claims: 39
A processor with a selector in the instruction-fetch data path. When the instruction fetcher fetches instructions from the instruction cache, and the cache hits, the selector delivers the instruction. When the cache misses, the selector provides a NOP instruction to minimize pipeline stalls.