# Triscend E5 Reconfigures Microcontrollers

*Flexible 8-Bit and 32-Bit Chips Combine Programmable Logic With CPU Core*

*by Jim Turley*

EMBEDDED PROCESSOR FORUM

All microprocessors are programmable, but some, it seems, are more programmable than others. That is the thinking behind Triscend's new programmable microprocessor, the E5, introduced at Embedded Processor Forum last month. The E5 combines popular CPU architectures with an array of field-programmable logic to create a customizable controller for low-end embedded applications. The concept has been tried before—not always successfully—but Triscend's approach has some unique features that may help the E5 get a foothold in future markets.

Triscend vice president Danesh Tavana hosted the company's coming-out party at the Forum and provided the first details of the chip's design. He and the company's other founders, Chris Balough and Stanley Yang, came from Xilinx, a background that colored the design of the E5. First samples of Triscend's chips won't be available until the beginning of next year, but Tavana believes that many 8-bit users will embrace the concept by 2001.

## 8032 Core Is the Same; Programmable Logic Isn't

Triscend's E5 is basically an 8032 microprocessor with some fixed peripherals and a large array of programmable logic, as Figure 1 shows. The CPU core is a licensed design, and the peripherals are compatible with the dozens of 8032 derivatives that are already available. The CPU runs at 40 MHz—quite fast for an 8-bit chip—and connects to the rest of the chip through a nonmultiplexed multimaster bus.

Where the E5 differs from other 8032-based microcontrollers, of course, is in its programmable logic. The first E5 chip is about 65% logic array, by silicon area. The reprogrammable SRAM-based logic is used to create additional peripherals on demand. The logic array also allows E5 developers to reallocate most of the chip's external pins to suit their printed-circuit board layout.

This ability to create "derivatives on demand" is Triscend's greatest strength, according to Tavana. Even with the dizzying assortment of 8032-based controllers already available through normal means, customers want to create still more variations for their own applications. Peripherals such as serial ports, timers, DMA channels, and decoders can be added, modified, and removed at will during development. Pinouts can be assigned for convenience.

Triscend is keeping up with the move to high-level, abstract design tools for logic development. Users can design with OrCad schematics or Synopsys logic synthesis. The company also provides a graphical tool that allows developers to drag the image of a timer/counter, UART, or address decoder onto a block diagram of the chip. Address, data, and control lines are automatically connected, and address header files are generated for programmers.

Triscend's business model calls for tiered pricing of peripheral designs. Several of the most basic peripherals (timers, FIFOs, and others) will be made available at no additional charge. Somewhat more complex subsystems (CAN controllers, $I^2C$ ports) will carry a licensing fee, and larger functions (DSP coprocessor, USB controller, PCI interface) will be more expensive.

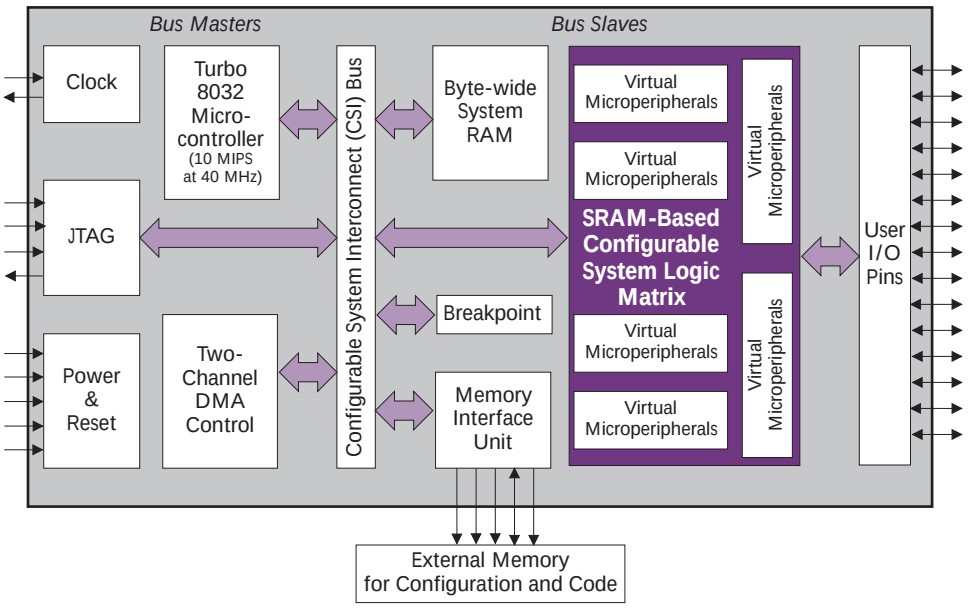



**Figure 1.** Triscend's E5 design is based on a fixed 8032-compatible core, some fixed peripherals, and a large array of programmable logic with which users can create additional peripherals.

## Options for Logic and SRAM

The first chip in the planned E5 family, the TE520, will have 2,048 "logic cells," each roughly equivalent to an Altera LE or one-half of a Xilinx XC4000-series CLB. The 520 thus provides about as much free logic as a Xilinx XC4013 or XCS30 FPGA. The 520 also has 16K of system RAM, above and beyond the chip's programmable logic.

| Product Family Name | Bit Width | Embedded Processor Core | Device | Logic Cells | RAM | I/O (max) |
|---|---|---|---|---|---|---|
| E5 | 8 | 40 MHz 10 MIPS 8032 | TE505S08 | 512 | 8K × 8 | 123 |
| | | | TE512S16 | 1,152 | 16K × 8 | 187 |
| | | | TE520S40 | 2,048 | 40K × 8 | 251 |
| | | | TE532S64 | 3,200 | 64K × 8 | 315 |

**Table 1.** Triscend anticipates producing four variations of its E5, with varying amounts of programmable logic and SRAM.

### Price & Availability

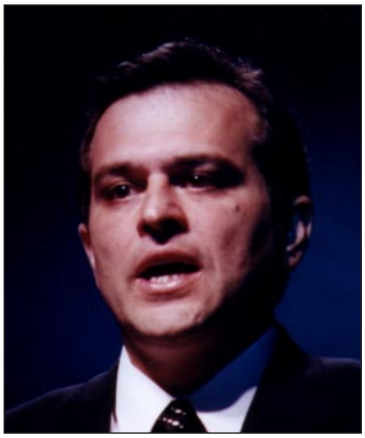
Triscend's TE520 will begin sampling in 1Q99. In 100-unit quantities, the 10-MHz TE520 will be priced at $55.

For more information, contact Triscend (Mountain View, Calif.) at 650.968.8668 or visit *www.triscend.com*.

As Table 1 shows, follow-on devices will have either more or fewer logic cells, SRAM, and I/O pins. All four devices will be offered in the same PQFP-208 package for pin-compatible upgrades; smaller or larger packages are also planned, as necessary.

Triscend is expecting first silicon of the 520 late this year; general sampling should begin in 1Q99, with production volumes in 2Q99. The parts are fabricated by UMC in its 0.35-micron, four-layer-metal CMOS process. The total die area of the 520 has not been disclosed.

Configurability doesn't come cheap. In small (100-piece) quantities, Triscend is asking $55 for the 520. This is a hefty $45 premium over run-of-the-mill 8032 microcontrollers from Philips, Intel, Dallas, or others. Tavana said Triscend is optimistic those prices can come down by 75% as the device moves to 0.25-micron and 0.18-micron production over the next four years. That would make the 520 a $14 part in 2002, still undoubtedly more expensive than its hardwired competitors.



MICHAEL MUSTACCHI

**Danesh Tavana of Triscend describes his company's configurable processor at the Forum.**

## ARM7TDMI Version in 1999

Looking ahead, Triscend is now designing an ARM7TDMI-based version of its configurable processors. Unlike the E5 family, these 32-bit processors will be built by Sharp in its 0.25-micron process. First samples are expected late in 1999.

A 32-bit variation will lure a different class of customer to Triscend. It will also make an interesting prototyping vehicle for potential ARM-based ASIC customers. The 32-bit chips will use the same style of configurable logic, so peripherals designed for the E5 should port transparently.

## Triscend Follows Motorola's Ghost

The E5 parallels the development of Motorola's ill-fated Core+ family of configurable processors (see MPR 2/16/98, p. 10). In Motorola's case, the Core+ parts were to have paired ColdFire with the company's fledgling FPGA architecture. Chips were due in 3Q98, but scant months before their arrival, Motorola pulled the plug on Core+ and the FPGA architecture it was to be based on (see MPR 7/13/98, p. 14).

The demise of Motorola's programmable processor was part of an austerity drive in the wake of dismal financial results. Also, the company's FPGAs weren't popular (or well known), casting doubt on the combined product.

As with Core+, the E5 is a package deal. Potential designers must be happy with both the processor and the logic architecture. Triscend has dealt with the first concern by selecting one of the most popular 8-bit CPUs available. Even if its audience is limited to current 8032 users, that's a large potential market for a small startup to pursue.

Triscend dealt with the second concern by optionally hiding the organization of the logic fabric from the user. Its drag-and-drop development tool is the closest many users might get to programming the logic matrix directly. Given that level of abstraction, Triscend could rework the fundamental FPGA architecture in future chips, and customers would be none the wiser.

## Convenience, Not Performance

But the fundamental problem with configurable processors remains. Is the combination of processor and logic under one roof significantly more valuable than the two apart? It certainly sacrifices customer choice, and if Triscend's early samples are any example, it's much more expensive. The fundamental advantages of the E5 are space savings, competitive performance (at least in 8-bit form), and the ability to produce custom derivatives on demand.

In the world of 8-bit microcontrollers, where cost is often the overriding concern, the E5's premium price seems hard to justify. On the other hand, microcontroller-based products show up in high-volume consumer applications (toys, audio components, remote controls) that are subject to short-term demand, regional differences, and customer whims. The ability to make product alterations on short notice without modifying PC boards (or even opening the box) could mean a lot in such high-pressure markets.

Ultimately, Triscend's customers will be paying for convenience. The E5 is a kind of insurance against unexpected product changes, delays, or regulatory requirements. Time to market is the most important "feature" of many embedded projects, not price, performance, or power consumption. On that ground, Triscend's tools—hardware and software—provide a lot of value. But as Motorola's example shows, that value proposition has a lot of challenges. M