Motorola PowerPC 8240 Gets PCI Bus

Hot on the heels of its PowerQUICC II announcement (see MPR 9/14/98, p. 12) Motorola has rolled out another high-end PowerPC for embedded systems. Like the recent 8260, the new PowerPC 8240 is based on Motorola's high-end 603e processor. Unlike the 8260, however, the new 8240 has full floating-point capability and a PCI bus interface.

Despite their similar part numbers, the 8240 and the 8260 are quite different beasts. Whereas the 8260 (PowerQUICC II) is a communications controller with a PowerPC thrown in for good measure, Motorola's new 8240 is a straightforward PowerPC processor with core-logic I/O and none of the serial channels of the 8260. Under Motorola's new four-digit part-numbering system, "8" indicates an integrated chip, and "2" identifies a G2 (603/604) PowerPC core; the last two digits are essentially random. This nomenclature leaves plenty of room for 740/750-based chips (83xx) and future G4-based devices (84xx).

The 8240 integrates core-logic functions that most embedded designers can use: namely, a DRAM controller, DMA channels, and a 66-MHz, 32-bit PCI bus interface. The DRAM controller handles 100-MHz synchronous DRAMs (SDRAMs) as well as the less costly EDO (extended data-out) and fast page-mode DRAMs. Its 64-bit-wide interface includes ECC for data reliability. The internal interrupt controller handles I_2O-style messaging, so the 8240 could conceivably be used in disk or networking subsystems.

Motorola is offering the 8240 processor at 200 and 266 MHz. Low-power customers can run the chip as slowly as 100 MHz, at reduced voltage, to save power. Typical power consumption at 2.5 V and 200 MHz is pegged at 3 W.

Motorola has set aggressive prices for its newest device. The 8240 will sell for $60 and $90 at 200 MHz and 266 MHz, respectively (both in 10,000-unit quantities), which is close to the price of the generic PowerPC 603e itself. Given the extra value of its DRAM and PCI controllers, the 8240 could quickly displace the 603e in the eyes of potential customers. Now that the 603e has left Apple's product line, its fall will be swift. The 8240 might finally lure loyal 68K customers away from the 68040 and 68060, which offer nowhere near the price/performance of the 8240 in systems that need floating point. —*J.T.*

Intel's i960VH Sprouts Single PCI Bus

Intel continues to push around the various ingredients in its i960 family, looking for tasty combinations. The latest dish from the Intel kitchens is the i960VH, a chip that lies somewhere between the i960JT and the i960RP on the 32-bit RISC menu.

The new 'VH processor is unique among i960 chips in having just one PCI interface. Intel's four R-series processors each have dual PCI buses (upstream and downstream) for I_2O applications. The other i960 incarnations, in contrast, have no PCI at all. With just one PCI bus, the 'VH is not really suitable for I_2O systems, but it could be attractive for the growing legions of PCI-based embedded systems. CompactPCI backplanes, for example, could take advantage of the 'VH, as could single-board systems that use PCI for I/O interconnect.

The new i960VH is based on the J-series core, which means the chip has a 16K instruction cache, a 4K data cache, 1K of on-chip SRAM, and runs at 100 MHz. Like Motorola's new PowerPC 8240 (see previous item), the i960VH has a DRAM controller, a two-channel DMA controller, and an I_2O-style messaging interface. The 3.3-V part is housed in a 324-contact PBGA (plastic ball-grid array) package.

The similarities between the i960VH and Motorola's 8240 are obvious. Both have PCI, DMA, DRAM control, I_2O support, and surface-mount packages. Intel's $45 asking price for the 100-MHz i960VH (in 10,000-piece quantities) is at least $15 cheaper than Motorola's price for the 8240, but the PowerPC chip runs twice as fast (200 MHz vs. 100 MHz), has a faster PCI bus (66 MHz vs. 33 MHz), a bigger data cache (16K vs. 4K), a wider memory bus (64 bits plus ECC vs. 32 bits), and an IEEE-754 floating-point unit.

Overall, the 8240 provides a better value for designers willing to spend the extra $15, not to mention better performance. Unless embedded designers have a requirement for i960 software compatibility—or an aversion to PowerPC—the i960VH appears to be just as overpriced and underpowered as the rest of the i960 family. —*J.T.*

Pentium/MMX Goes Embedded

Now that the chip has outlived its usefulness in the notebook PC market, Intel's Pentium/MMX is now officially an embedded microprocessor. The company has shifted responsibility for the chip from its mainstream desktop PC group to its embedded division in Chandler (Arizona), lowered prices, and extended the production life of the part by several years.

The Pentium/MMX (called the "Low Power Pentium Processor with MMX Technology" in Intel parlance) is the same 0.25-micron Tillamook chip that powers laptop PCs. As such, it has a 64-bit bus, full FPU, dual 16K caches, and the famous x86 software compatibility. The chip is offered in 166-MHz and 266-MHz speed grades and two packages, including a new, low-profile BGA package.

The use of the term "low power" is somewhat optimistic; the chip typically dissipates 2.9 W at 166 MHz and 5.3 W at 266 MHz, according to Intel. In 1,000-unit quantities, the Pentium/MMX sells for $51 (166 MHz) or $104 (266 MHz), well below its former PC prices. At these prices, the Pentium/MMX is a relatively good value. Although there

are many RISC processors that provide superior price/performance, none of them can match the wealth of software, development tools, and infrastructure that Pentium brings with it. —*J.T.*

ARC Getting Full—30 Licensees Aboard

Two by two, Argonaut RISC Cores (*www.risccores.com*) is slowly accumulating licensees of its 32-bit RISC architecture. Like its better-known down-river rival ARM, ARC has made a good business out of designing and licensing microprocessor cores to ASIC developers and semiconductor vendors. At last count, ARC had signed 30 licensees, close to the number in the ARM band.

Although the two have many similarities, ARM and ARC follow somewhat different strategies. ARC prefers to license its wares directly to users, that is, to developers or semiconductor makers that will use the ARC core in their own products. Significantly, ARC also allows—encourages, in fact—its licensees to modify and improve on the ARC instruction set and architecture. This configurability is unusual in the processor intellectual property industry and gives ARC a leg up over ARM in many accounts.

Although ARC does not identify most of its licensees, Texas Instruments, Fujitsu, and newcomer eCryption Technology are among them. ARC's relatively inexpensive licensing fees and flexible and extensible architecture are its most attractive features. At this rate, ARC may soon run out of companies to which it can license its wares. —*J.T.*

NEC Multiplies V830 Media Performance

At last month's Embedded Processor Forum, NEC unveiled the V830R, a new DSP- and media-enhanced member of the V830 family of processors. The V830 and V831, introduced last year, are moderate-performance devices running at 100 MHz (see MPR 6/2/97, p. 22 and 8/4/97, p. 10). The V83x parts already include some basic DSP features, such as a 32 × 32-bit multiplier, multiply-accumulate instructions, saturating arithmetic, and on-chip SRAM.

The new V830R, which is upward-compatible with the V83x devices, adds extensive DSP and media-processing capabilities through the addition of a 64-bit-wide single-instruction, multiple-data execution unit. While many MCUs and CPUs have received SIMD retrofits in recent years, NEC's approach is slightly different. The V830R uses a VLIW-like mechanism to issue up to one integer and one SIMD-unit instruction per cycle. In contrast, Intel's SA-1500 provides a separate SIMD coprocessor with its own thread of control, while Intel's MMX CPUs and their ilk dynamically schedule varying numbers of SIMD and regular instructions in each cycle.

The V830R SIMD unit contains 32 64-bit registers and can perform up to four 16-bit or eight 8-bit operations in parallel. Beyond the usual complement of arithmetic and logical operations, the SIMD unit supports multiply-accumulate (MAC) and a few other specialized operations, such as absolute value of the difference of two operands. Saturating arithmetic and unbiased rounding are also supported. If 16-bit accumulation is used, four 16-bit MAC operations can be performed in parallel. If 32-bit accumulation is desired, only two MACs can proceed at once.

While the SIMD unit performs number crunching, the integer unit can perform address calculations or control operations. However, choreographing the simultaneously issued SIMD and integer instructions will prove a challenge to programmers, who will likely be forced to work in assembly language for maximum performance.

To alleviate some of the performance-sapping alignment complications that often arise when applying SIMD processing to DSP algorithms, NEC includes instructions that support unaligned memory accesses. Once started, a series of unaligned 64-bit accesses proceeds at a rate of one 64-bit word every two cycles.

The new SIMD unit will give the V830R a significant boost in per-cycle DSP power over the earlier V83x devices. In addition, NEC is targeting a 200-MHz clock rate for the new device, twice that of its predecessors.

The V830R targets multimedia applications such as audio and video compression as well as more traditional DSP applications. According to NEC, V830R first silicon is expected by the end of 1998. The device will be packaged in a 208-pin PQFP and is projected to dissipate 1.3 W at 200 MHz, using split 2.5/3.3-V supplies. It will be fabricated in NEC's 0.25-micron, four-layer-metal process and contain 3.6 million transistors. —*Jeff Bier, BDTI*

iReady Picked Up by Toshiba, Seiko

Two companies have announced their first products based on the Internet "tuner" from iReady (see MPR 10/6/97, p. 14). Toshiba and Seiko Instruments have both demonstrated working silicon that incorporates iReady's hardware-only networking stack: an interface chip and an LCD display, respectively.

Toshiba's sample Internet tuner is a general-purpose Internet interface device with an x86 bus to a host processor, an SRAM interface, serial and parallel ports, and a keyboard controller, all in a 208-lead PQFP package. Samples are available now for ¥2,000 (about $17).

Seiko is integrating the iReady technology a little more closely with its products. The company will produce a family of LCD modules with the iReady tuner already integrated. Seiko plans a family of small, text-only displays with an integrated network stack along with a second line of larger, quarter-VGA (320 × 240) panels with network, e-mail, and Web functions.

Both licensees, as well as iReady (*www.ireadyco.com*), believe that these products will first appear in digital cellular telephones, possibly as early as next quarter. Although iReady's approach to Internet connectivity is certainly unusual, at least some major companies seem willing to gamble on it. —*J.T.* M