AUDIO/VIDEO

3-D graphics drive speeding buses. Bus architectures are allowing midrange PCs through high-end workstations to put super high-quality graphics on the map. Vincent Biancomano, *Computer Design*, 9/98, p. 75, 3 pp.

MMX speeds machine-vision algorithms. Many core requirements of multimedia processing overlap with those of industrial machine vision, so it's natural that the latter also benefit from this new computational capacity. John Lecky, Imaging Technology; *Personal Engineering*, 10/98, p. 35, 8 pp.

BUSES

VME maintains its ironclad position as a high-end bus architecture. Its heritage and infrastructure are unmatched, and new schemes such as VME320 and vPCI are paving the path to the future. Jeff Child, *Electronic Design*, 9/14/98, p. 59, 7 pp.

DEVELOPMENT TOOLS

Various paths taken to accelerate advances in HW/SW codesign. EDA vendors are working hard to develop and make available technology that will help you to design and verify system ASICs with hardware and software content. Barbara Tuck, *Computer Design*, 9/98, p. 24, 2 pp.

In-circuit emulators. The need to peer inside of embedded code has spawned a great number of debugging products. All have their own strengths and weaknesses, their unique features and price points. Jack G. Ganssle, *Embedded Systems*, 10/98, p. 75, 7 pp.

DSP

Diverging architectures for digital signal processing. In the past couple of years, DSP architectures have become much more interesting, with a number of vendors announcing new architectures that are completely different from preceding generations. Jennifer Eyre, Berkeley Design Technology; *RTC*, 9/98, p. 17, 3 pp.

DSPs expand in power and specialization. The year has seen a new DSP architecture from a startup company, the merging of integer and floating-point architectures by a major player, and a host of specialized devices. Rodney Myrvaagnes, *Electronic Products*, 10/98, p. 49, 4 pp.

Analog signal processing functions go digital. Data-converter performance coupled with DSP techniques have enabled new system architectures that are more flexible and reliable, and less expensive. Paul Hendriks, Analog Devices; *Computer Design*, 7/98, p. 50, 4 pp.

Breaking Nyquist. It is generally believed that digital signal processing cannot remove or identify aliased signals. But this isn't exactly true. There is a method for identifying and removing aliases after sampling, and it's even possible to identify and measure signals above the sampling rate. Gerard Fonte, *Circuit Cellar*, 10/98, p. 30, 5 pp.

MEMORY

Monolithic IC "mirrors" complete disk drive. Beating the design challenges of marrying memory and logic achieves a disk-on-a-chip at a cost equivalent to raw flash. Jeff Child, *Electronic Design*, 10/12/98, p. 65, 4 pp.

PERIPHERAL CHIPS

Ripple regulator takes off on Merced's command. As microprocessor design rapidly jumps from 32- to 64-bit architectures, the amount of power a processor can dissipate has led to a demand for complex, low-voltage power controllers that push the performance envelope to new heights. Ashok Bindra, *Electronic Design*, 10/1/98, p. 33, 3 pp.

PROCESSORS

Architecting modern embedded CPUs. Performance isn't the only consideration in architecting an embedded processor. Meeting design reuse, debug, power consumption, software, and operating-system needs are also important considerations. Phil Bourekas, IDT; *Computer Design*, 9/98, p. 58, 6 pp.

PicoJava: a direct execution engine for Java Bytecode. A small, flexible microprocessor core, PicoJava directly executes Java bytecode instructions and provides hardware support for other essential functions of the Java virtual machine. Harlan McGhan and Mike O'Connor, Sun Microsystems; *Computer*, 10/98, p. 22, 9 pp.

Comm-fusion engine bridges multiple protocols at near-gigabit speeds. It slices, it dices, it makes lovely julienne ATM packets. Handling ATM, Ethernet, and TDM traffic, Motorola's PowerQUICC II, a dual-CPU, multi-PHY communication processor does it all—and does it well. Lee Goldberg, *Electronic Design*, 9/14/98, p. 34, 6 pp.

PROGRAMMABLE LOGIC

System-class CPLDs zip along at flank speeds of 110 MHz. The high-density ispLSI family's arsenal packs 840 macrocells, delivers up to 43,750 PLD gates, and sports 312 I/O pins. Dave Bursky, *Electronic Design*, 9/14/98, p. 48, 5 pp.

Advanced CPLD architectures challenge FPGAs, gate arrays. With 1,000+ gates in their arsenals, complex programmable logic devices (CPLDs) have become essential building blocks and prototyping tools for many digital systems. Dave Bursky, *Electronic Design*, 10/1/98, p. 78, 7 pp.

SYSTEM DESIGN

Improve your chance of design success with advanced packaging. The latest evolution of EDA tools and design processes bridges the gap between IC and PC-board designers. Cheryl Ajluni, *Electronic Design*, 10/12/98, p. 79, 6 pp.