by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,748,950

Method and apparatus for providing an optimized compare-and-branch instruction
Issued: May 5, 1998
Inventors: James E. White, et al.
Assignee: Intel
Filed: March 20, 1997
Claims: 12
An instruction sequencer that detects a compare-and-branch instruction and executes it as a regular compare instruction. On the next cycle the sequencer translates the instruction into a branch instruction and provides it for execution by one of the execution units. The branch is executed, either taken or not taken, and normal program flow continues.

5,748,936

Method and system for supporting speculative execution using a speculative lookaside table
Issued: May 5, 1998
Inventors: Alan H. Karp, et al.
Assignee: HP
Filed: May 30, 1996
Claims: 20
In a processor with speculative execution, a speculative lookaside table stores information about deferred exceptions. Labels attached to predicates in a predicate register file index a speculative lookaside table. On a speculative exception, the speculative lookaside table is updated. Deferred exceptions are detected and handled when the processor reads the corresponding entry in the speculative lookaside table during an explicit or implicit check operation.

5,748,932

Cache memory system for dynamically altering a single cache memory line as either branch target entry or prefetch instruction queue, based upon instruction sequence
Issued: May 5, 1998
Inventors: Korbin S. Van Dyke, et al.
Assignee: AMD
Filed: January 25, 1995
Claims: 10
A microprocessor with a branch target cache (BTC) and two instruction-prefetch circuits. A control mechanism fetches instructions from a sequential prefetcher until a conditional branch is detected. If the branch is predicted taken, the second prefetcher prefetches instructions from the predicted target address. If the branch was mispredicted, the pipeline is flushed and the sequential fetcher is restarted.

5,745,725

Parallel instruction execution with operand availability check during execution
Issued: April 28, 1998
Inventor: Robert John Simpson
Assignee: SGS-Thomson
Filed: July 12, 1996
Claims: 21
A mechanism for allocating instructions to different execution units in a processor. Each instruction is tagged with a sequence number, its assigned execution unit, and its sequential predecessor's execution unit. If an instruction requires the result of its immediate predecessor, that result may be accessed (before retirement of the preceding instruction) from the execution unit registers of the execution unit given by the predecessor tag.

5,742,804

Instruction prefetch mechanism utilizing a branch predict instruction
Issued: April 21, 1998
Inventors: Tse-Yu Yeh, et al.
Assignee: IDEA (Intel/HP)
Filed: July 24, 1996
Claims: 12
A microprocessor, and methods of operation, where a branch predict instruction is used to speculatively fetch the target instructions of a conditional branch, based on the predicted outcome of the branch. The execution of the instruction causes no user-visible architectural state change.

5,742,840

General-purpose, multiple-precision parallel operation, programmable media processor
Issued: April 21, 1998
Inventors: Craig Hansen, et al.
Assignee: MicroUnity
Filed: August 16, 1995
Claims: 11
An execution unit with a programmable, extended mathematical element and a multiprecision arithmetic unit coupled to a data path. The arithmetic unit is capable of dynamic partitioning based on the width of the data on the data path at a point in time. The width of the data for the partitioning is defined to be less than or equal to the width of the data path.

OTHER ISSUED PATENTS

5,748,937 *Computer system that maintains processor ordering consistency by snooping …* M