## Hitachi Upgrades SuperH/DSP Combination

At the recent Embedded Processor Forum, Hitachi product manager Jim Slager discussed the latest version of his company's hybrid CPU/DSP architecture, SH3-DSP. As with the existing SH-DSP architecture (see MPR 12/4/95, p. 10), the SH3-DSP merges a SuperH microprocessor with an integrated DSP coprocessor. The hybrid chip executes a single instruction stream from a unified instruction set, but it can carry out more than one operation at a time. Specifically, SH3-DSP chips can execute one integer and one DSP operation in parallel with loads and stores. The first SH3-DSP chip is sampling now at 133 MHz; production is scheduled for 2Q99.

As the name suggests, the SH3-DSP design is based on a third-generation SuperH (SH-3) processor core (see MPR 3/6/95, p. 12), such as that used in the SH7708. Internally, SH3-DSP chips have four buses: one for instructions, two for data transfers between the single register file and the dual ALUs, and an extra data bus for DMA transfers. As with Hitachi's earlier SH-DSP designs, on-chip memory is divided between cache and X/Y data memories, an organization familiar to DSP programmers.

The first incarnation of the SH3-DSP architecture, the SH7729, has a 16K unified cache and another 16K of X/Y data memory. The chip's MMU makes it compatible with Windows CE, as are most SH-3 chips. A memory controller, four-channel DMA controller, timers, serial interfaces, and A/D and D/A converters round out the peripheral mix. The 3.3-million-transistor device measures 53 $mm^2$ in Hitachi's 0.18-micron (effective) three-layer-metal process. At 133 MHz and 1.8 V, the chip consumes just 200 mW, according to Hitachi. According to the MDR Cost Model, the SH7729 costs $12 to build in a 208-lead LQFP package.

During his presentation, Slager described several target applications for the SH7729, including GSM phones, Windows CE handhelds with wireless communication ability, and voice-over-IP (VoIP) networking. Recently, Hitachi proudly announced a deal with network leader Cisco for just such a system.

VoIP has become a hot capability, as networking companies jockey to compete with traditional telephone providers, catalyzing the development of DSP-enabled microprocessors. Hitachi has made a strong start in this area, faring better than ARM's Piccolo or the MIPS MDMX extensions. Motorola's AltiVec was also designed, in part, for such applications and will certainly give Hitachi a run for its money at the high end (see MPR 5/11/98, p. 1). SuperH's tight code size and low power consumption, along with Hitachi's demonstrated ability to mass-produce inexpensive parts, will all help the company distinguish itself amid the confusing whirl of merged microprocessor and DSP chips. —*J.T.*

## MIPS Exposes the Family Jewels

MIPS Technologies (*www.mips.com*) took its first significant step as an independent company, unfolding its roadmap for future CPU cores and altering its licensing and distribution strategy. Henceforth, MIPS will be offering its cores in both synthesizable and hand-packed form, and not necessarily just to its seven licensed partners.

The company's new roadmap includes three embedded MIPS cores, identified by the code names Jade, Opal, and Ruby. Jade, the smallest one of the group, combines the aging R3000 microarchitecture with some R4000-style features, much as IDT did with its recently announced RC32364 processor (see MPR 6/1/98, p. 12). The first Jade-based chips are expected to appear in 2Q99.

Opal is a midrange 64-bit design reminiscent of the R5000. MIPS is coy about Ruby, except to say that it will deliver "industry-leading performance." We expect it will be a superscalar design. The timelines for Opal and Ruby were not disclosed, although they are further out than for Jade.

All three cores will initially be available (to MIPS licensees) in a hard-layout format. This is a change from standard MIPS procedure, where the company licensed the instruction-set architecture only and left circuit design largely to the discretion of the individual licensees.

Synthesizable versions of the cores are planned to follow the hard macros by a few months. This is also a first for MIPS but a growing trend in the industry.

Finally, the company revealed that it plans to distribute the new cores beyond just its inner circle of licensed semiconductor manufacturers (IDT, LSI, NEC, NKK, Philips, QED, and Toshiba). While the company is probably not ready to license directly to small, private engineers, it is considering approaching "market leaders" in specific areas. Such an approach might put MIPS at odds with its licensee partners, leading to friction, but it may be the only way to survive against firms like ARM, ARC, and Lexra as the CPU core market heats up. —*J.T.*

## SandCraft Shows Superscalar SR1 MIPS Core

ASIC designers with a penchant for MIPS cores have been confronted with a plethora of products lately, and SandCraft intends to prolong the dilemma. At the recent Embedded Processor Forum, SandCraft president and founder Norman Yeung lifted the veil from the SR1, SandCraft's two-way superscalar 64-bit MIPS core for high-end ASIC development. The SR1 promises to overtake other MIPS cores from LSI Logic and compete against MIPS Technologies' own Opal and Ruby designs (see previous item).

The SR1, code-named Montage, is only the second design to emerge from SandCraft (*www.sandcraft.com*), the small design firm that codeveloped NEC's high-end VR5464 processor (see MPR 3/9/98, p. 1). SandCraft does not have a

MIPS license, restricting its customer base to those companies that do.

The SR1 is intended for high-end relatively general-purpose applications. It boasts a total of six execution units, including two integer units, a dedicated multiply-accumulate unit, a load/store unit, and a branch unit. The sixth execution unit, the FPU, is microarchitecturally separate from the others. It resides on the other side of the MediaLink Bus, a SandCraft spin on the standard MIPS coprocessor interface. This bidirectional 64-bit connection allows up to eight coprocessors to run independently of the main execution units, a feature particularly useful for long-latency operations. During his presentation, Yeung indicated that future SandCraft designs could include DSP and/or SIMD media-processing units on the MediaLink bus.

After instructions are fetched into a 16-deep instruction buffer, they are sorted into an 8-deep issue queue and dispatched, two at a time, to the six execution units. Instructions can be dispatched out of order, with results posted to an 8-deep result buffer. Results are committed in order (up to two per cycle) as MIPS compatibility dictates. This approach decouples fetching, dispatching, executing, and committing instructions and, Yeung stated, maximizes the number of instructions per clock (IPC) by minimizing dependencies and the effects of branch misprediction.

As with ARM10 (see MPR 11/16/98, p. 14) and some other recent core designs, the instruction and data caches are an intrinsic part of the core. In the case of the SR1, these caches are each 16K in size, and two-way set-associative; they allow locking and, in the case of the data cache, support both write-back and write-through updates. Interestingly, both caches also have parity protection (byte parity for the data cache; 32-bit word parity for the instruction cache). Cache parity is a relative rarity on any microprocessor and particularly unusual for a CPU core.

The SR1 is distributed as a hard macro rather than as a synthesizable design. This goes somewhat counter to recent trends, but it allows (and requires) SandCraft to work more closely with the core's users and avoids the necessity of using standard and compatible synthesis tools.

The SR1 core design is complete, and the finished macro will be available before mid-1999, according to Yeung. The core is expected to run at about 250 MHz in a 0.25-micron process and measure about 25 $mm^2$, most of which is cache. In a 0.18-micron process, the SR1 should reach 400 MHz, shrink to about 14 $mm^2$, draw about 1 W, and hit 800 Dhrystone MIPS, according to the company.

SandCraft has a tough road ahead of it. Although the MIPS architecture has proved hugely popular in recent years, there's also no shortage of suppliers filling that demand, and MIPS itself is about the enter the fray with its own CPU core macros. Without access to the MIPS brand name, SandCraft may have trouble marketing its independent designs against those of MIPS, which owns the architecture and has established relationships with the chip vendors. —*J.T.*

## Mentor Scores IBM PowerPC Cores

Tool-maker Mentor Graphics has acquired a license to sell two of IBM's embedded PowerPC processor cores to its ASIC customers. Beginning next year, Mentor customers will be able to design ASICs using the PowerPC cores. Previously, PowerPC-based ASICs were possible only through IBM's own semicustom business.

Mentor will offer the PowerPC 401 and 405 cores. The 401 is a simple, low-end core first announced in 1996 (see MPR 6/17/96, p. 9) that appears in IBM's inexpensive 401GF processor chip. The 401GF is a low-power scalar processor that runs at under 100 MHz and sells for less than $15 in quantity. It competes primarily with low-end MIPS devices.

The PowerPC 405 is a new core, first announced by IBM at the recent Embedded Processor Forum (see MPR 10/26/98, p. 26). At 200 MHz and up, the 405 is a relatively high-performance core, with additional multiply-accumulate (MAC) features.

IBM's deal with Mentor highlights a growing trend toward making cores directly available to chip designers, not just semiconductor foundries. Last week, MIPS Technologies made a similar announcement, revealing a roadmap for synthesizable cores that will be licensed directly to major hardware developers. ARM, too, has recently begun licensing synthesizable versions of its ubiquitous ARM7 design. Clearly, the industry trend points downward, shifting design decisions away from the semiconductor vendors and into the hands of product developers. —*J.T.*

## AMD K6E Is Officially Embedded

Like Intel, AMD has officially handed off responsibility for its former PC processor to its embedded group (see MPR 11/16/98, p. 10). In AMD's case, the chip in question is the original K6, now called K6E. Also like Intel's Pentium/MMX, the chip is completely unchanged from its halcyon days as a mainstream PC processor.

In 1,000-unit quantities, the 0.35-micron K6E is priced at $81 (233 MHz) or $84 (266 MHz), modest discounts from the days of PC pricing. The tiny $3 difference in their prices reflects the minuscule difference in performance between these two speed grades. As before, these K6 processors have their full floating-point unit, complete MMU, 64-bit bus, and Socket 7 compatibility.

AMD's price for its 266-MHz chip is a good $20 (25%) cheaper than Intel's price for an equivalent 266-MHz embedded Pentium/MMX. Intel offers slower and cheaper versions of Pentium/MMX at 166 and 200 MHz, with prices that undercut AMD's, starting at just $51. AMD's K5 processor slipped quickly and quietly under the surface, having never seen the light of an embedded day. AMD's embedded customers can now switch from the speedy 486DX5-133 directly to the K6, if they're willing to completely redesign their hardware (but maintain that all-important software). Looking ahead, new integrated chips based on the K6 might start appearing early in 1999. —*J.T.* M