QED Demonstrates Improved PCI I/O

Alpine Processors Automate Transactions Between Memory, PCI, and Processor

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EMBEDDED PROCESSOR FORUM

With the same devotion many processor designers reserve for the CPU core, QED has developed an I/O structure that promises to deliver twice the bus bandwidth of competing designs. At the recent Embedded Processor Forum, QED design manager Bill Fisher cleared the mists surrounding Alpine, the code name for the company's latest pair of processors.

The Alpine chips (officially, the RM5710 and RM5720) don't advance the state of the art in CPU design but instead remove bus bottlenecks. Both attach QED's RM5261 processor core (see MPR 8/3/98, p. 11) to a 64-bit, 133-MHz SDRAM interface, a low-speed, 8-bit local peripheral bus, and one ('10) or two ('20) 66-MHz PCI buses. From a software perspective, the Alpine chips are no different from the RM5231, '61, or '71. To a hardware engineer, the difference is like night and day.

The RM5710 and '20 will begin sampling in 2Q99, with production scheduled for 4Q99; QED (*www.qedinc.com*) has not yet announced pricing for these parts.

Floating in the Buffer Pool

What makes the Alpine chips interesting is their internal I/O management. The chips' PCI buses, local buses, and memory interfaces all have their traffic coordinated through a shared "buffer pool," as shown in Figure 1.

The buffer pool is organized as sixteen 32-byte entries. Each entry is tagged with its physical address, somewhat like a 16-entry cache with very long lines. There are five ports into the pool, with one each for the CPU, the memory controller, and each of the two PCI interfaces. The fifth port is shared among the relatively low speed ports: DMA, scratchpad, and local bus. All transactions among these ports are broken into two unconnected transfers: a write into the buffer pool and a read from the buffer pool. After a transaction is initiated, the target of the transfer retrieves its data from the buffer pool as if it had come directly from the source.This split-transaction model isolates the latency of, say, the PCI bus from that of the memory, allowing each bus master to release its bus as soon as possible.

The buffer pool runs at the CPU frequency—300 MHz in the initial chips—so the initial latency for CPU transactions is the same as for an L1 cache hit. Bandwidth is the real issue here, and Fisher showed some evidence during his presentation that Alpine can transfer data to or from the PCI bus at 2× or 3× the rate of an equivalent RM5261 processor using a separate dual-PCI controller, such as Galileo's GT-64120. Transactions initiated by a PCI master to the processor's memory controller also showed a significant 20%–50% increase in bandwidth.

Concurrency extends to the chips' SDRAM controller, which is divided into three independent state machines managing three concurrent accesses. Accesses are interleaved, based on their relative priority (reads before writes, refreshing banks of memory are bypassed, CPU before PCI, etc.), to make the most of finite memory bandwidth.

Alpine's designers started with a high-level description of the RM5261, onto which they grafted the buffer pool and autonomous I/O interfaces. The total silicon area for the 5710 and '20 (which are actually the same die in different packages) is 56 mm^2, or about 25% bigger than the RM5261 these are based upon. The part has not yet taped out, but QED is hopeful that 0.25-micron sample parts will pop from foundry partner IBM's fabs around the spring of 1999.

Better PCI Ready for More I/O

The RM5710 and '20 join a small cadre of processors (such as Motorola's MPC8240 and Intel's i960VH) with PCI buses. Like QED, these competitors have knitted PCI into existing processors to expand customers' I/O capabilities. A single PCI interface gives easy access to Ethernet and other I/O controllers. Even with dual PCI buses, the RM5720 is not equipped for I_2O applications; it's more of a central processor with access to high-end PCI peripherals.

QED invested a lot of effort in Alpine's buses, bandwidth, and buffers, an investment that will pay off as future chips roll off the QED drawing boards. Alpine is just the bedrock for an inevitable line of new integrated controllers. When more peripheral controllers are added and bandwidth really becomes an issue, the value of QED's solid integration work will really peak. M

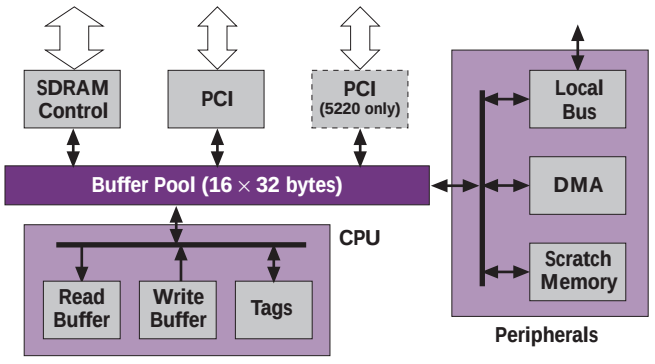

Figure 1. QED's RM5710 and RM5720 processors manage their bus transactions through a shared buffer pool, which has five ports into the processor, PCI, DRAM, and other peripheral controllers.