*by Rich Belgard, Contributing Editor*

*The following U.S. patents related to microprocessors were issued recently. Please send e-mail to* belgard@umunhum.stanford.edu *with comments or questions.*

## 5,758,142

*Trainable apparatus for predicting instruction outcomes in pipelined processors*
Issued: May 26, 1998
Inventors: Scott McFarling et al.
Assignee: Digital (Compaq)
Filed: May 31, 1994
Claims: 31
The invention is a predictor that chooses between two or more subpredictors. The predictor includes a subpredictor that uses one algorithm to predict an action and another subpredictor that uses a different algorithm. Each subpredictor predicts the same action. The invention is such a predictor to choose between predictions provided by the subpredictors. The invention can be used to predict outcomes of branches, cache hits, prefetched instruction sequences, etc.

## 5,758,141

*Method and system for selective support of nonarchitected instructions within a superscalar processor system utilizing a special access bit within a machine state register*
Issued: May 26, 1998
Inventors: James Allen Kahle et al.
Assignee: IBM
Filed: February 10, 1996
Claims: 8
A method and system permitting support of nonarchitected instructions within a superscalar processor. A special access bit within the system machine-state register is set during initiation of a program with nonarchitected instructions. Each time a nonarchitected instruction is decoded, the special access bit is examined. The nonarchitected instruction is executed if the special access bit is set; otherwise an illegal instruction trap is generated.

## 5,758,115

*Interoperability with multiple instruction sets*
Issued: May 26, 1998
Inventor: Edward Colles Nevill
Assignee: ARM
Filed: June 7, 1995
Claims: 12
A data processor having a processor core for executing instructions of a predetermined set of instruction sets. The processor also has data memory for storing programs, a program counter for indicating the address of a next instruction, and a control that uses one or more least-significant bits of the program counter to determine which of the multiple instruction sets the core is to execute.

## 5,754,878

*CPU with DSP function preprocessor having pattern recognition detector that uses table for translating instruction sequences intended to perform DSP function into DSP macros*
Issued: May 19, 1998
Inventors: Saf Asghar et al.
Assignee: AMD
Filed: March 18, 1996
Claims: 18
A microprocessor that includes a general-purpose CPU, such as an x86-processor core, and a DSP. The CPU also includes an intelligent DSP function preprocessor that examines x86 opcode sequences to determine whether a DSP function is being executed. The function preprocessor recognizes instruction sequences that implement DSP functions. If the function preprocessor determines that a DSP function is being executed, the preprocessor maps the opcodes to a DSP macroinstruction that is provided to the DSP.

## 5,754,812

*Out-of-order load/store execution control*
Issued: May 19, 1998
Inventors: John Gregory Favor et al.
Assignee: AMD
Filed: January 26, 1995
Claims: 83
Scheduler logic that tracks the relative age of stores with respect to a particular load (and of loads with respect to a particular store) and allows a load/store execution controller to hold younger stores until the completion of older loads (and to hold younger loads until completion of older stores). Address-matching logic allows a load/store execution controller to avoid load/store (and store/load) dependencies. Propagate-kill scan chains supply the relative age indications of loads with respect to stores (and of stores with respect to loads).

## OTHER ISSUED PATENTS

**5,758,117** *Method and system for efficiently utilizing rename buffers to reduce dispatch unit stalls in a superscalar processor*
**5,758,112** *Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction*
**5,758,051** *Method and apparatus for reordering memory operations in a processor* M