TeraGen Reveals 8-Bit Threaded Processor

Continuing the new trend toward turning the lowly 8-bit microprocessor on its ear, startup TeraGen (*www.tera-gen.com*) has revealed that it is developing an 8051-compatible chip that emulates not only the entire 8051 instruction set but the peripherals (a la Scenix and Triscend) as well. Furthermore, the TeraGen part will run at an unheard-of speed of 200–250 MHz, according to company founder (and former Intel and Cirrus executive) George Alexy. TeraGen's unnamed microprocessor will begin sampling around the middle of 1999. Pricing has not been announced.

TeraGen takes RISC and VLIW concepts to extremes, at least for an 8-bit microprocessor. The chip internally consists of several "microthread engines." Each microthread engine executes a proprietary VLIW instruction set, using local on-chip ROM. The contents of the ROM determine the features and native instruction set of the microthread engine. Coordination among the microthread engines is managed by an internal hardware scheduler.

Each microthread engine can be assigned by the scheduler to execute program code or to emulate the functions of a peripheral, such as a UART or a timer. The greater the number of microthread engines per chip, the greater the number of peripherals the chip can emulate simultaneously. One or more microthread engines are used for emulating the CPU. In the initial TeraGen parts, this CPU is an 8051, although that too is configurable. Because each microthread engine executes at 200 MHz or more, Alexy says each one can easily emulate the peripherals found on a typical 5-MHz microcontroller.

The advantage of this fast-but-dumb approach is configurability. Depending on the contents of the local ROM, TeraGen chips can be designed to emulate virtually any instruction-set architecture, regardless of register organization, word length, or RISC/CISC heritage. Given enough microthread engines, Alexy believes his chips could just as easily replace 16-bit and 32-bit processors, with or without peripherals. Chips could also be customized for a new instruction set or to fix annoying features of existing instruction sets. It's all a matter of changing the ROMs.

The other advantage is manufacturing cost. Initial samples of the TeraGen chip are only 60% of the size of an equivalent 8051, including peripherals, in the same 0.5-micron process. Furthermore, 90% of the die area is RAM, ROM, or data path, with very little complex control logic. Nor does the chip contain any microcode (in the usual sense). In all, TeraGen's performance scales readily with process improvements and delivers good circuit density.

TeraGen's business model is to both license the technology to others and market chips under its own label. The first licensee will be signed in 1Q99, and the second in 2Q99, according to the company. TeraGen's own chips are set to debut in the second half of 1999. —*J.T.*

Lexra Rolls Out Second MIPS Core

Renegade MIPS developer Lexra (*www.lexra.com*) has doubled its product line with a new MIPS-like processor core, the LX4180. The '4180 improves on the initial LX4080 by adding hardware support for 16-bit multiply-accumulate (MAC) instructions, an EJTAG debug interface, and MIPS-16 code compression (see MPR 2/16/98, p. 13). The core will begin shipping to licensees within 1Q99, according to Lexra.

The new LX4180 also improves clock frequency to 155 MHz through a shift to 0.25-micron design rules. (The unusual frequency is convenient for SONET/OC-3 applications.) Lexra says the core (without caches) measures just 2.75 mm^2 in 0.25-micron CMOS and consumes 175 mW (typical). The design is fully static and uses a single clock edge, making it easier to design and debug using commonly available tools. The core's local bus now supports a synchronous protocol, as well as an asynchronous one. As with the original Lexra core, this one doesn't support the MIPS-I unaligned-transfer instructions (which are trapped and emulated), due to legal entanglements.

Lexra's "up-front pricing" is a change from the arcane deals offered by most IP companies. The single-project fee starts at $325,000, with royalties at around at $0.40 per chip, decreasing with volume. Both synthesizable and physical formats will be available.

Lexra provides its customers with hooks into the processor's microarchitecture, allowing designers to add their own instructions and/or coprocessors as desired, something the official MIPS licensees frown upon as nonstandard. Lexra's prices and flexibility are attractive to a whole new underclass of aspiring ASIC designers. On the other hand, the company cannot offer the level of support that companies like MIPS, Toshiba, and LSI Logic can. On the whole, Lexra's few hardy customers seem happy with that tradeoff. —*J.T.*

Toshiba, NEC Make 10-Year Ruby Investment

Two longtime MIPS licensees, NEC and Toshiba, have both re-upped their licenses for another 10 years, according to MIPS Technologies. The two have also licensed MIPS's forthcoming Ruby processor core, the first companies to publicly do so, although details of Ruby itself are not expected to be announced until the end of 1999.

Ruby will become the new top of the line for MIPS as it rolls out its three new processor cores over the next few years (see MPR 12/7/98, p. 10). MIPS has said only that Ruby will be a 64-bit MIPS-V design with "high-performance graphics extensions," presumably a reference to MDMX. Coincident with the NEC/Toshiba announcement, MIPS revealed a new tidbit of information: Ruby is expected to deliver more than 1,000 Dhrystone MIPS and run at speeds in excess of 1 GHz, although no development schedule was given for reaching either of these milestones. —*J.T.*