by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,768,575

Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control …
Issued: June 16, 1998
Inventors: Harold L. McFarland, et al.
Assignee: AMD
Filed: March 13, 1995
Claims: 19
Superscalar methods and processor hardware for translating CISC instructions into RISC instructions, issuing and executing the RISC instruction out of program order, and committing the instruction results in program order.

5,764,529

Method and apparatus for automatic frequency and voltage selection for microprocessors
Issued: June 9, 1998
Inventors: Louis Bennie Capps, Jr., et al.
Assignee: IBM
Filed: December 23, 1996
Claims: 8
A method and hardware for use in a microprocessor by which a required operating clock speed and voltage level are made available on power-up. The circuit using the microprocessor reads the information from the microprocessor and sets the clock speed and voltage levels to those required.

5,761,516

Single chip multiprocessor architecture with internal task switching synchronization bus
Issued: June 2, 1998
Inventors: Michael D. Rostoker, et al.
Assignee: LSI Logic
Filed: May 3, 1996
Claims: 27
A data-transfer bus and processor-synchronization bus interconnect multiple processors, a memory controller, and an I/O controller on a single chip. The processor-synchronization bus lets one processor cause the other to perform a task by generating an interrupt and passing the required parameters.

5,761,506

Method and apparatus for handling cache misses in a computer system
Issued: June 2, 1998
Inventors: Richard L. Angle, et al.
Assignee: Bay Networks
Filed: September 20, 1996
Claims: 5
A multistreaming processor, and methods of operation, whereby an operation of a first task is scheduled to a functional unit. If the operation causes a cache miss, the operation is rescheduled to a memory function unit, and a different task is scheduled in the first function unit.

5,761,492

Method and apparatus for uniform and efficient handling of multiple precise events in a processor by including event commands in the instruction set
Issued: June 2, 1998
Inventors: John Susantha Fernando, et al.
Assignee: Lucent Technologies
Filed: May 7, 1996
Claims: 44
A pipelined microprocessor and methods for providing precise interrupts. The processor detects multiple simultaneous events and enters event operations, selecting the highest-priority event first, to the processor in place of the next instruction(s). The event operations then flow through the pipeline logic in a manner similar to instructions.

5,761,470

Data processor having an instruction decoder and a plurality of executing units for performing a plurality of operations in parallel
Issued: June 2, 1998
Inventor: Toyohiko Yoshida
Assignee: Mitsubishi
Filed: December 18, 1995
Claims: 18
A processor that uses a format field to specify the number of operation fields of an instruction code and the order of execution of operations. The data processor is similar to a VLIW data processor; however, the operation fields can specify more types of operations and the instruction code may be packed.

OTHER ISSUED PATENTS

5,768,610 *Lookahead register value generator and a superscalar microprocessor employing same*
5,765,206 *System and method for emulating a segmented virtual address space by a microprocessor that provides a non-segmented virtual address space*
5,765,037 *System for executing instructions with delayed firing times*
5,764,940 *Processor and method for executing a branch instruction and an associated target instruction utilizing a single instruction fetch* M