Infineon's TriCore Tackles DSP

Superscalar Hybrid Competes With Other Hybrids, DSPs

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In late 1997 Siemens Semiconductors announced its entry into the field of hybrid DSP/microcontrollers, the TriCore core (see MPR 11/17/97, p. 13). Among the current crop, TriCore is one of the few hybrids that isn't a DSP retrofit of an existing microcontroller design. Siemens hoped to avoid legacy constraints by creating a completely new architecture that borrows from many architectural traditions but is bound to none.

For example, TriCore has a 32-bit data path, like most high-performance microcontrollers, and uses superscalar execution, like a high-end CPU. In addition, TriCore incorporates considerable DSP-oriented hardware and instructions. With this combination, Siemens is aiming to embed TriCore in a variety of applications, including high-performance disk drives, communications systems, and automotive engine-management systems.

At last October's Embedded Processor Forum, Siemens' Rod Fleck revealed that TriCore-based chips have already been fabricated and are being used to verify the architecture and to test TriCore's tool suite. Current test chips operate at 33 MHz with a 2.5-volt supply in a 0.35-micron process; Siemens expects to offer 80-MHz TriCore-based chips in a 0.25-micron process by mid-1999. Siemens has announced that all future TriCore chips will use a slightly modified version of the initial architecture, making the current test chip something of an orphan. This unusual move may have come

as a result of Siemens' drive to get silicon as quickly as possible, even as TriCore was undergoing final architectural adjustments. The revised architecture, designated TriCore V1.2, will provide a per-cycle DSP performance boost of about 10%, according to Siemens.

Earlier this month, Siemens Semiconductors announced a name change to Infineon Technologies following its spin-off from parent company Siemens AG. Infineon is the latest participant in the spin-off name game, following in the footsteps of Conexant (formerly Rockwell Semiconductor) and Lucent (formerly part of AT&T). Infineon plans to use TriCore in its own application-specific chips and to offer TriCore for licensing, an unusual strategy that it is also pursuing with its recently introduced high-end DSP core, Carmel (see MPR 12/28/98, p. 18).

This strategy may be attractive to many OEMs, which can use off-the-shelf TriCore-based chips during development and initial production and then migrate to more cost-effective core-based ASICs for volume production. Infineon has not yet announced any TriCore licensees, but it recently disclosed that it will be working closely with design startup Seagull Semiconductor (Israel) to develop additional IP modules for TriCore. At Embedded Processor Forum, Infineon hinted at the possibility of a floating-point version of TriCore in the future. If this hint becomes a reality, TriCore may become the first licensable floating-point DSP core.

TriCore's target applications require substantial DSP muscle, and Infineon claims that the processor is equal to the task. BDTI recently completed an independent evaluation of TriCore; this article is based on that analysis and focuses on TriCore's DSP-oriented features and performance rather than on its microcontroller capabilities.
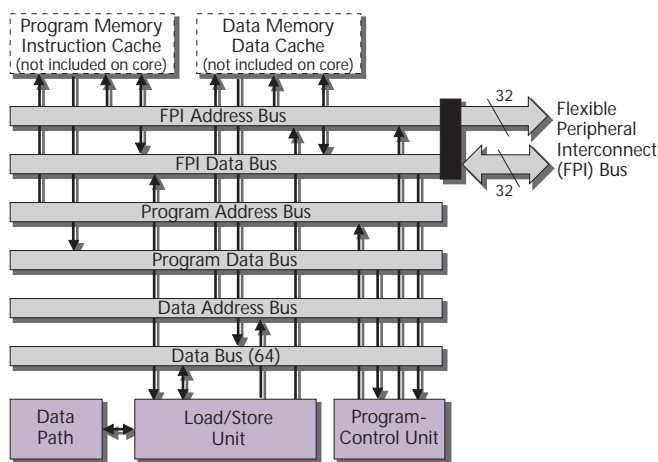
It's an MCU, It's a DSP, It's …

TriCore couples an MCU-like RISC-based load/store design with a DSP-like Harvard memory architecture, as Figure 1 shows. The core's dual address buses are each 32 bits wide, and its program and data memory buses are 64 bits apiece. The core itself does not contain any memory, leaving the ASIC designer to customize the memory configuration.

TriCore's superscalar architecture is built around a 32-bit fixed-point data path, a load/store unit, and a program-control unit. TriCore can execute up to three instructions per cycle—one data-path instruction, one load/store instruction, and one instruction that specifies a loop. Thus, achieving the peak instruction-execution rate requires that data-path instructions and load/store instructions be carefully paired.

TriCore's data path provides sixteen 32-bit address registers and sixteen 32-bit data registers. Two consecutive

Figure 1. Simplified block diagram of the TriCore architecture. TriCore is three-way superscalar and includes a data path, a load/store unit, and a program-control unit, each of which can execute one instruction per cycle.

data registers can be concatenated to form a 64-bit extended register. Most DSP processors provide accumulator registers that contain extra bits (called guard bits) to prevent overflow during a series of multiply-accumulates. TriCore does not provide explicit support for guard bits, but a few instructions can use the upper 16 bits of a 64-bit extended register as guard bits.

Data loads and stores are performed as single bits, bytes, or 16-, 32-, or 64-bit words. With the exception of bit and byte accesses, which can be performed at any memory location, all data accesses must address a 16-bit-aligned memory location. TriCore's support for single-bit accesses, mainly of interest in control-oriented code, is not found on any commercially available DSP processor. TriCore can perform either one load or one store per instruction cycle; on an 80-MHz TriCore, the maximum on-core data-memory bandwidth is thus 640 MBytes/s.

TriCore's limitation of one data access per clock cycle contrasts with the capabilities of most DSP processors, which can typically retrieve at least two separate data words while executing instructions within a tight loop. Although TriCore can retrieve up to four contiguous 16-bit data words in a single data access, the four words are routed to a single register rather than to separate registers. Programmers may need to unroll loops, because TriCore does not allow the programmer to specify an offset into a 64-bit register to access and operate on its constituent 16-bit words.

Multiple Multiplication Options

To meet the DSP demands of its target applications, TriCore supports a number of specialized multiply and multiply-add operations as well as SIMD (single instruction, multiple data) additions and multiplications. Using its SIMD capabilities, TriCore can execute two 16-bit multiplies with single-cycle throughput—twice the multiplication throughput of today's midrange DSP processors.

TriCore's specialized multiply-add capabilities include instructions that allow one or two 16-bit multiplication results to be left-shifted by 16 bits and then added to the contents of a 64-bit extended register, effectively implementing a 64-bit accumulator with 16 guard bits. Table 1 summarizes TriCore's multiply and multiply-add/subtract operations.

Unlike most DSP instruction sets, TriCore's explicitly supports 32-bit multiplies. Throughput for wide multiplications, however, is significantly reduced; 32-bit multiplies, have a two-cycle latency and (for reasons that are not entirely clear) a throughput of one multiplication every three cycles. TriCore's ability to perform both 16-bit and 32-bit fixed-point multiplies allows the programmer to trade off top speed and maximum precision as needed.

TriCore provides a Flexible Peripheral Interconnect bus (32-bit address, 32-bit data) to connect to off-chip peripherals and (with the help of a special external memory-interface unit, called the External Bus Controller) to off-chip memory.

TriCore uses a mixed 16/32-bit instruction set. DSP-oriented instructions are 32 bits wide; 16-bit instructions are aimed at control-oriented processing. TriCore programmers can freely intermix the two instruction widths without setting mode bits.

Although TriCore's instruction set is more regular and orthogonal than that of the average DSP, optimizing assembly code on a SIMD superscalar processor carries its own difficulties. For example, the programmer must expend significant effort to pair data-path and load/store instructions so execution units aren't kept waiting, and effective use of SIMD often requires special optimization and data-organization techniques that take some getting used to. Of course, programmers can throw their hands up and rely on the compiler—but that means leaving some (maybe a lot) of the processor's performance on the table, which few DSP programmers are willing to do.

TriCore uses a four-stage pipeline consisting of fetch, decode, execute, and write-back stages. The pipeline depth is comparable to that of most mainstream DSP processors, and considerably shorter than that of some of the latest high-end DSPs, such as TI's VLIW TMS320C6xxx. On many DSP processors, certain combinations of instructions can cause pipeline stalls, and instructions must be carefully arranged to avoid them. Compared with most DSP processors, TriCore experiences fewer such pipeline stalls, since nearly all TriCore instructions (except taken branches and multiplications) complete in a single instruction cycle.

Other DSP Goodies

To generate the data-access patterns common in digital-signal processing, TriCore supports a number of DSP-oriented addressing modes, including register-indirect with pre- and post-increment, indexed addressing, circular (modulo) addressing, and bit-reversed addressing (useful for unscrambling the inputs or outputs of some FFT algorithms). TriCore also supports zero-overhead hardware looping.

TriCore includes a coprocessor, directly connected to its register file, that is capable of performing powerful bit-interleaving functions. For example, in BDTI's convolutional-

Multiply Widths	Multiply-Add, Multiply-Sub Widths
$16 \times 16 \rightarrow 16$*	$16 \times 16 + 32 \rightarrow 16$*
Dual $16 \times 16 \rightarrow 16$*	Dual $16 \times 16 + 32 \rightarrow 16$*
$16 \times 16 \rightarrow 32$	$16 \times 16 + 32 \rightarrow 32$
Dual $16 \times 16 \rightarrow 32$	Dual $16 \times 16 + 32 \rightarrow 32$
–	$(16 \times 16) \ll 16 + 64 \rightarrow 64$[†]
–	$(16 \times 16 + 16 \times 16) \ll 16 + 64 \rightarrow 64$[†]
$32 \times 32 \rightarrow 32$[§]	$32 \times 32 + 32 \rightarrow 32$[§]
$32 \times 32 \rightarrow 64$[§]	$32 \times 32 + 64 \rightarrow 64$[§]

Table 1. TriCore multiply and multiply-add/subtract options. All multiplication operations support both integer and fractional operands, unless otherwise noted. All multiplication operations use signed operands and provide optional saturation, unless otherwise noted. *results rounded from 32 bits to 16 bits. [†]signed integer values only; saturation not supported. [§]signed or unsigned

Price & Availability

TriCore test chips are available now. Infineon expects to have TriCore V1.2 chips in mid-1999, with a projected price of $15.

Development tools are available from Green Hills Software and from Tasking; these companies have also announced that they will port their real-time operating systems to TriCore. For further information, you can visit the Web at *www.tri-core.com.*

encoder benchmark (based on the IS-54 standard for digital cell phones), TriCore is able to perform the needed bit interleaving in one instruction cycle per 32-bit word. In contrast, most DSP processors chew through 40–50 cycles to do the same thing. Although the coprocessor is not considered an integral part of the core, Infineon states that it will be included in every TriCore-based chip and is also available to core licensees. Infineon has alluded to the possibility of providing other coprocessors in the future.

Running the Numbers

In an effort to get an accurate reading on TriCore's DSP performance, BDTI's DSP benchmarks were implemented and hand-optimized for TriCore in assembly language. The benchmark results indicate that Infineon has a legitimate claim to having fielded a hybrid architecture that crunches numbers like a DSP; as the example benchmark results presented in Figure 2 illustrate, an 80-MHz TriCore will have no trouble holding its own against TI's 100-MHz midrange DSP, the TMS320VC549.

It is interesting to note, however, that TriCore's performance relative to the 'C549 is not as much faster as one might expect, given TriCore's dual-MAC capabilities (the 'C549 can execute only one MAC per cycle). The shortfall
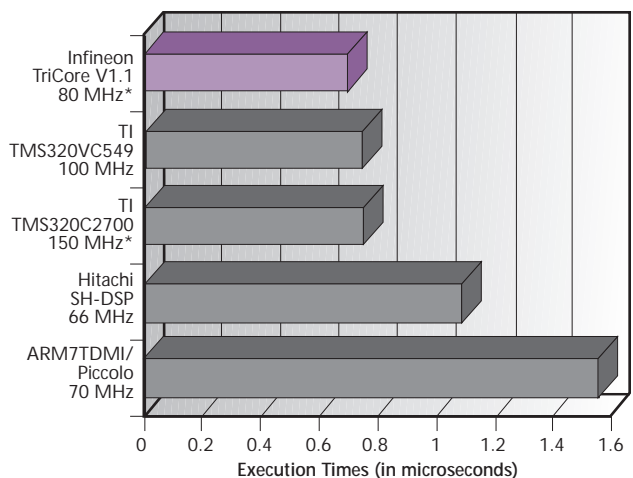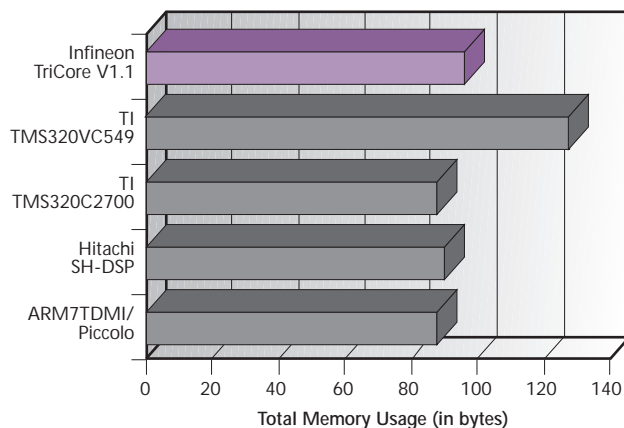

Figure 3. Total memory usage for BDTI's control-oriented benchmark. (Source: BDTI)

results from performance penalties incurred due to TriCore's data-alignment restrictions.

TriCore's superscalar architecture and SIMD capabilities give it an edge over the other hybrids shown here, in terms of per-cycle efficiency, providing a reminder that higher clock speeds (or MIPS ratings) don't necessarily mean better performance. Like all processors with SIMD capabilities, TriCore exhibits better performance on algorithms with high data parallelism.

As would be expected, TriCore's instruction set provides efficient support for control-oriented tasks by including a wide range of logical and bit-manipulation operations, several of which are not normally seen on DSP processors. These features, combined with TriCore's mixed-width instruction set, serve to keep code size small. This fact is evidenced by the processor's memory-usage results on BDTI's control-oriented benchmark, as Figure 3 shows. In general, TriCore's code density can be expected to be comparable to that of other hybrids and better than that of most DSP processors.

TriCore appears well equipped to tackle the computing requirements of applications with even moderate-to-heavy DSP requirements, and its single-core, single-tool-chain programming model may be appealing to system developers who dread the prospect of dealing with separate DSP and microcontroller software-development environments.

TriCore's strong DSP performance gives it the potential for success in DSP-intensive applications; it remains to be seen, however, whether the architecture will fulfill that potential and become widely adopted. Any new architecture needs substantial infrastructure to be successful, and TriCore is no exception. Infineon may have to overcome the obstacle of being the new kid on the block where DSP is concerned, particularly since its new name isn't yet a household word. Ⓜ

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Figure 2. Execution times (in microseconds) for BDTI's LMS adaptive FIR filter benchmark. *projected (Source: BDTI)