Media, Signal Processing Strong at Forum

Architecture Increasingly Divorced From Manufacturing in Embedded World

by Jim Turley

Next month's Embedded Processor Forum will include 19 different chip announcements from more than a dozen different companies, but there's surprising similarity surrounding some of the presentations. Digital signal processing, media processing, and process-independent core designs are recurring themes in the May conference.

High performance is also in evidence, with four presenters showing off their new high-end chips for embedded systems. Even in this realm, however, the emphasis is on nonstandard enhancements to the instruction set as much as on high clock rates and long pipelines.

High-End Chips Still Boast ISA Extensions

At the high end, Intel will detail its second-generation StrongArm core, under design since the 1998 acquisition of Digital Semiconductor. Also, IBM and Motorola will jointly pronounce upon Book E, the much-rumored embedded extensions to the PowerPC architecture (see MPR 10/27/97, p. 10). QED's unnamed 64-bit MIPS processor will flaunt its copper interconnect, while IBM will show off its PowerPC 750 (G3) with as-yet-undisclosed enhancements.

Sun's UltraSparc-IIe crosses the line between media processing and mainstream processing, adding both DSP and media extensions to the well-known SPARC architecture. SPARC has been a quiet but consistent player in embedded applications, accounting for about three million embedded units in 1998, or about 1.2% of the 32-bit embedded total. Other media-processing announcements center around chips with extensions intended for upcoming television set-top boxes and similar platforms. Likewise, Hitachi will show off its latest SuperH processor with its 3D-geometry extensions.

DSP Talks Split Between Cores and Chips

Three companies seem to have converged, both technically and temporally, on similar solutions. Processor-core vendors ARC Cores, ARM, and Lexra will all divulge the first details of their DSP extensions to their respective 32-bit CPU designs. The fact that all three companies have devoted considerable time and resources to this issue highlights the importance of signal processing in the ASIC business. Exactly how all three have addressed the problem will likely influence potential buyers' decisions for many years.

This will be ARM's second go at DSP extensions (see MPR 11/18/96, p. 17). Lexra and ARC Cores, on the other hand, have never had DSP extensions to their processors and will be announcing their enhancements for the first time.

Low Power a Key Advance for New DSP Chips

True DSP processors will also be in evidence at the Forum, with three separate announcements. The three, from Texas Instruments, STMicroelectronics, and DSP Group, advance the state of the art in high-end or low-power DSP chips. TI and ST, in particular, are vying for the low-power crown, with both companies' parts flirting with 1-V power supplies. DSP Group will reveal its latest generation of monosyllabic arboreal DSP cores, Teak.

ASIC Design at the Core and Integration Levels

ASIC and system-on-a-chip issues get heavy play at the Forum, with three announcements centered around licensed IP for customer-designed processors. MIPS Technologies will show off initial details of Jade, the first of its "family jewels" announced late last year (see MPR 12/7/98, p. 10). SandCraft, an independent design house working on high-end MIPS processors, will pull the wraps off the SR1-GX, a graphics-enabled spin-off of the SR1 microprocessor core that debuted at last year's Forum (see MPR 12/7/98, p. 10). Newcomer Tensilica is scheduled to show off XTensa, an unusual new configurable processor that's synthesized from a user-defined script.

Chip-design issues will also be the focus of a trio of announcements from Motorola, IDT, and TeraGen. Each company is taking a different approach to mixing CPU cores and peripherals. Whether through internal buses, gaskets, or circuit-level configurability, these companies are trying to slash development time and still make all their building blocks work together. A panel discussion that follows the presentations will delve into these issues further.

Dual Keynotes Place Consumers Over Technology

Keynote presentations will open each of the two main days of the conference. Author and consultant Don Norman will give his views on human-centered design; Scott Smyers of Sony Research Labs will talk about how digital systems are reshaping consumer electronics. Both talks, plus several of the Forum's new technology announcements, emphasize the way nontechnical consumers are driving the very technical decisions of how—and what—embedded engineers should be designing.

Evening affinity sessions will explore Java acceleration and benchmarks and present a survey of embedded designers' plans and wishes. All in all, the four-day conference promises to be an interesting forum for news, views, and opinions. M

The second annual Embedded Processor Forum will be held in San Jose (Calif.) May 3–6. For more information, or to register, visit www.MDRonline.com/epf.